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Atelier B has turned 20 – ABZ 2016 Linz

Presentation · May 2016

DOI: 10.13140/RG.2.2.33148.16000

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Thierry Lecomte
ClearSy System Engineering

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**Atelier B
has turned twenty**

Thierry Lecomte |
ABZ 2016
Linz



**Atelier B
User Manual**

Atelier B
manuel Utilisateur
Version 4.4
• Développement logiciel
• Modélisation système
• Validation formelle de données



Agenda

What happened during the last 20 years ?

Focus on some aspects:

- Modelling
- Proving
- Generating code

Not a raw description of the tool

More how its usage has evolved

Driven by projects

Atelier B initially developed by Fernando Mejia

◆ Development funded for Driverless metro in Paris (L14)

◆ First customer: University of Sherbrooke

◆ METEOR released

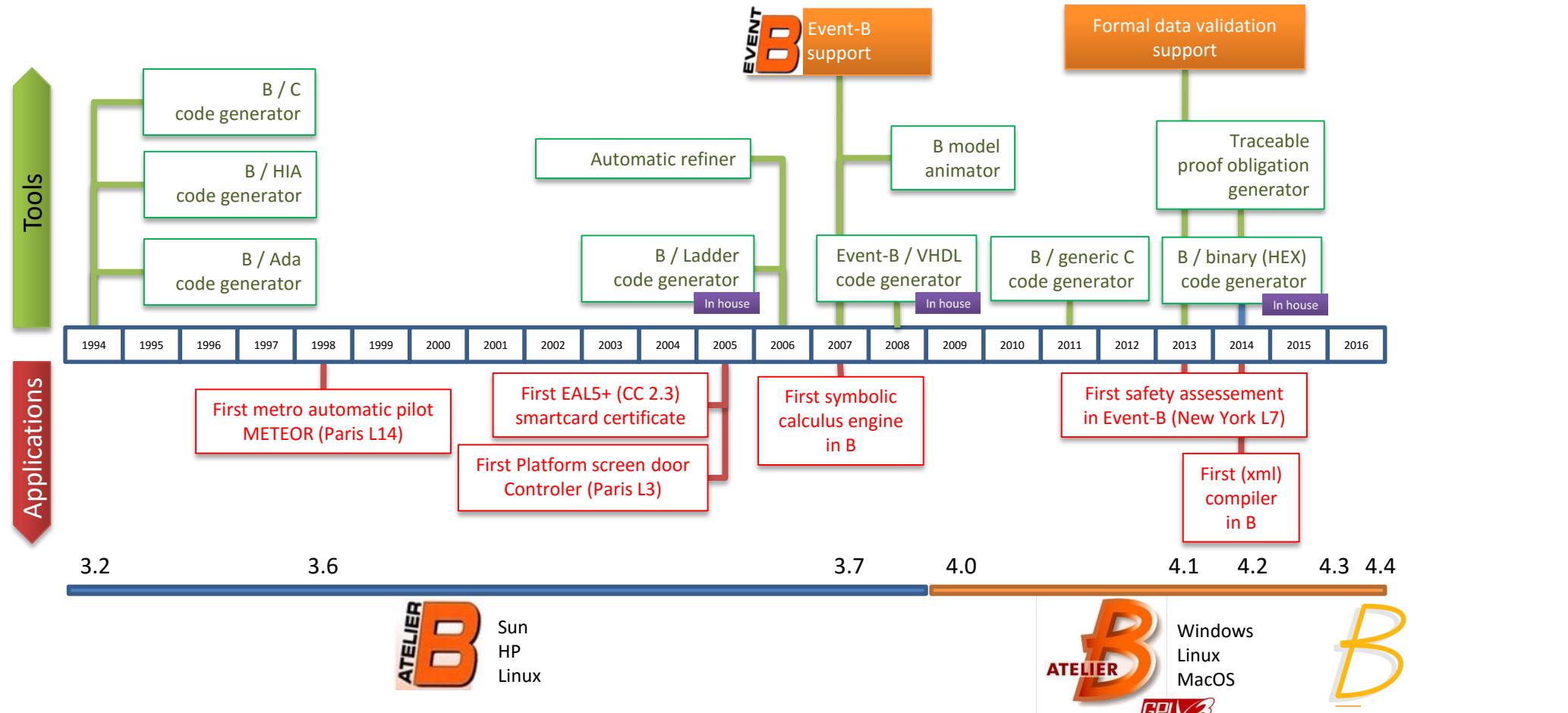
◆ Creation of ClearSy (full ownership)



MATRA

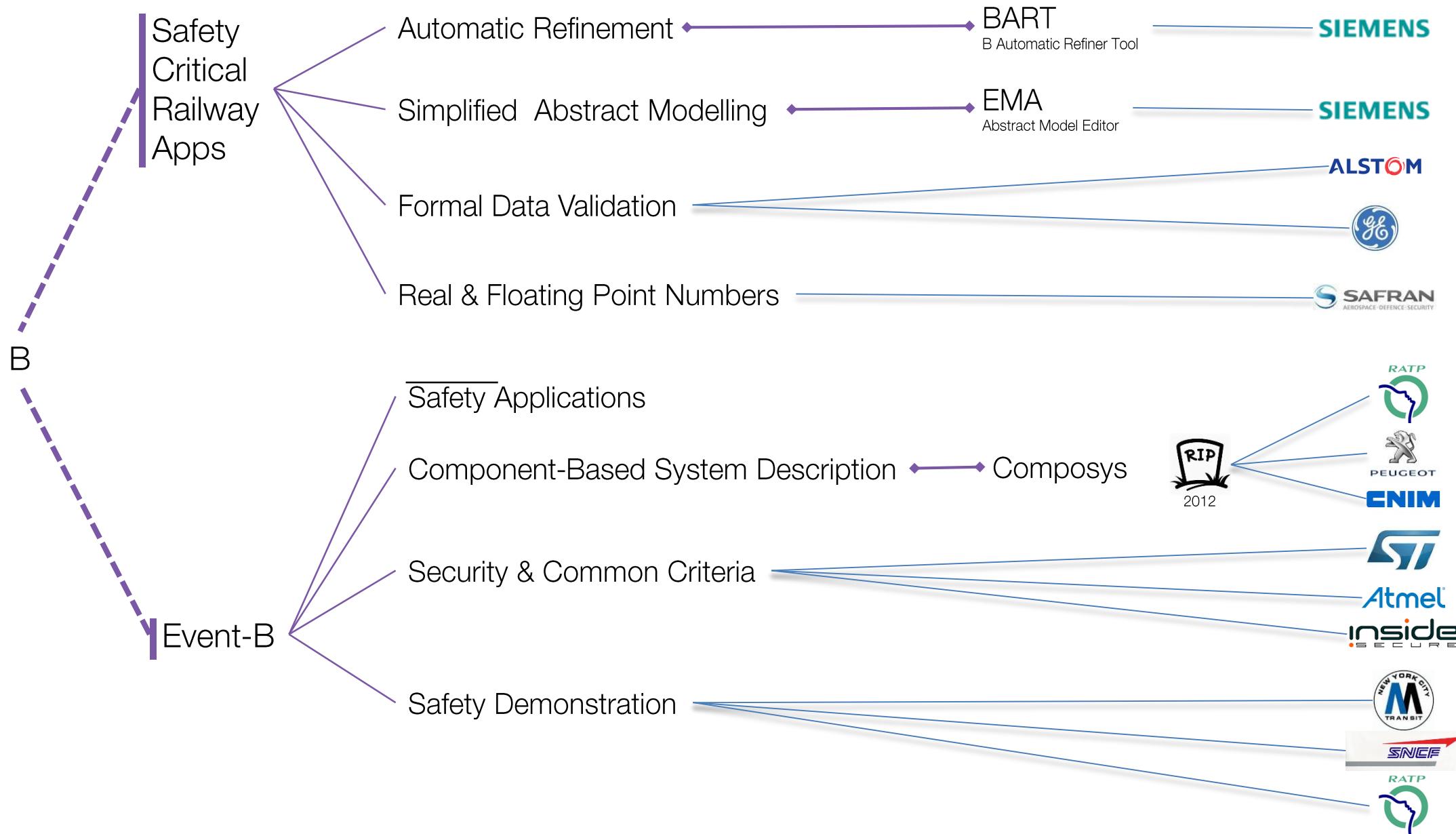


◆ Atelier B Community + Maintenance 



Modelling

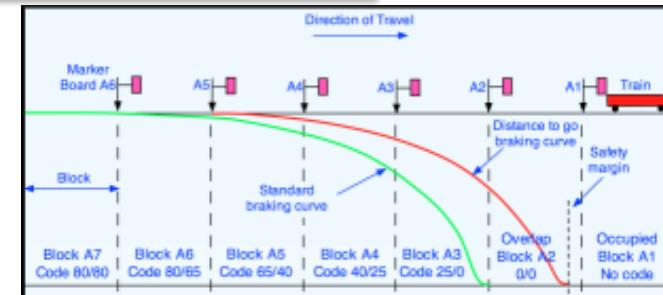
Modelling Random Walk



Safety Critical Railway Applications

≡ Reduce intervals between trains (from 120s to 90s / 75s)

- Passive security not sufficient (power off)
- Active security is required (trains have to brake when emergency)

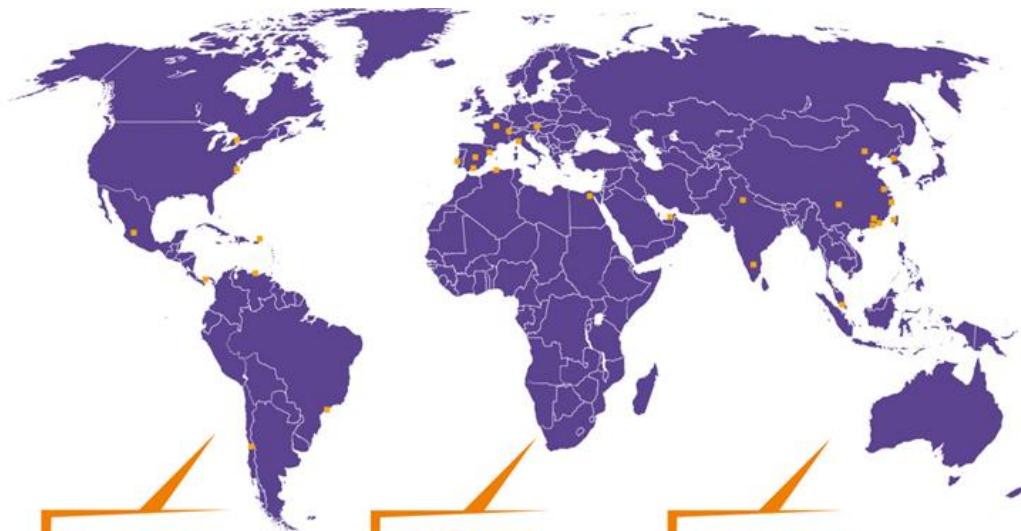


Braking curves

≡ B instead of program proof for

- Embedded software (Automatic Train Pilot)
- Localization: graph-based algorithms
- Energy control: integer arithmetic (braking curve)
- Emergency braking: Boolean predicates
- Trackside software (Interlocking)

≡ +30% automatic metros in the world



B initial success is due to urban women fertility

Confirm / Deny ?

NEW YORK
SAN JUAN
MEXICO
CARACAS
SANTIAGO
SAO PAULO
PANAMA
TORONTO

LAUSANNE
MILANO
BARCELONA
MADRID
LISBON
ALGIERS
CAIRO
BUDAPEST
PARIS
MALAGA
DUBAI

BENGALORE
DELHI
SEOUL
BEIJING
SHANGAI
HONK-KONG
SINGAPOUR
NINGBO
TAICHUNG
KUNMING
SHENZHEN
GUANGHOU

Safety Critical Railway Applications

Top level implementation

- Imports 55 components
- Specify top level one-cycle function:
 - Compute location, manage kinetic energy, control PSD, trigger emergency braking, etc.

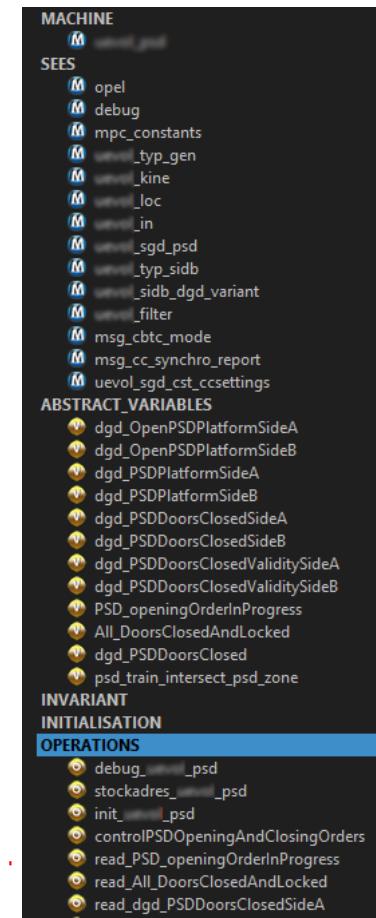
Metrics

- 233 machines, 50 kloc
- 46 refinements, 6 kloc
- 213 implementations, 45 kloc
- 3 000 definitions
- 23 000 proof obligations (83 % automatic proof)
- 3 000 added user rules (85 ?? % automatic proof)

Platform Screen Doors

- Top component: 12 variables 14 operations
- 10 components, 2 kloc specification, 2kloc implementation
- Connection with I/O through basic machines

Modern Automatic Train Protection Software
(2015)

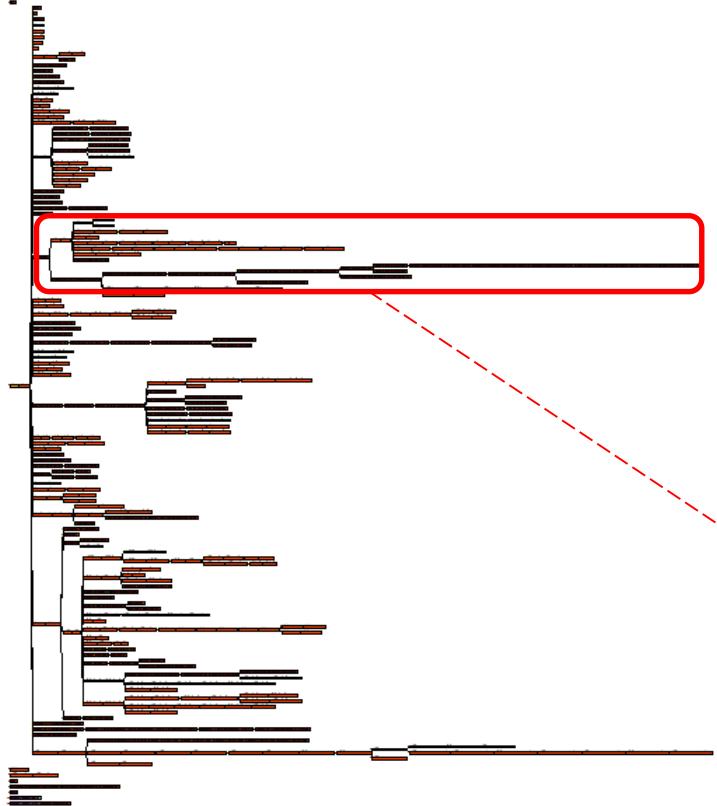


Safety Critical Railway Applications

Biggest function: Localization
where is the train ?

Post-condition of one operation:
variables become such as ...

root



Modern Automatic Train Protection Software
(2015)

```
variables :(types &
properties &
properties_train &

(loc_trainLocated = TRUE =>
  0 <= loc_locationUncertainty
  & kine_kineInvalid = FALSE
  & loc_train_track /= {}
  & first(loc_train_track) = loc_ext2Block |-> oppositeDirection(loc_ext2Dir)
  & !ii.(ii : 1..size(loc_train_track)-1 => loc_train_track(ii) : dom(sidb_nextBlock))
  & !ii.(ii : 1..size(loc_train_track)-1 => sidb_nextBlock(loc_train_track(ii)) = loc_
  & #aa.(aa : 1..size(loc_train_track) & prj1(t_block,t_direction)(loc_train_track(aa))

  & loc_rearBlock = { c_cabin1 |-> loc_ext2Block, c_cabin2 |-> loc_ext1Block, c_none |-
  & (loc_rearBlock = c_block_init
    => loc_rearDir=c_up)
  & ( not (loc_rearBlock = c_block_init)
    => loc_rearDir = { c_cabin1 |-> oppositeDirection(loc_ext2Dir), c_cabin2 |-> o
  & loc_rearAbs = { c_cabin1 |-> loc_ext2Abs, c_cabin2 |-> loc_ext1Abs, c_none |-> 0
  & loc_frontBlock = { c_cabin1 |-> loc_ext1Block, c_cabin2 |-> loc_ext2Block, c_none |
  & loc_frontDir = { c_cabin1 |-> loc_ext1Dir, c_cabin2 |-> loc_ext2Dir, c_none |-> d
  & loc_frontAbs = { c_cabin1 |-> loc_ext1Abs, c_cabin2 |-> loc_ext2Abs, c_none |-> a
  ))
```


Safety Critical Railway Applications

B model + tags (PRAGMAS)

Coverage

The screenshot shows the Atelier B interface with several windows:

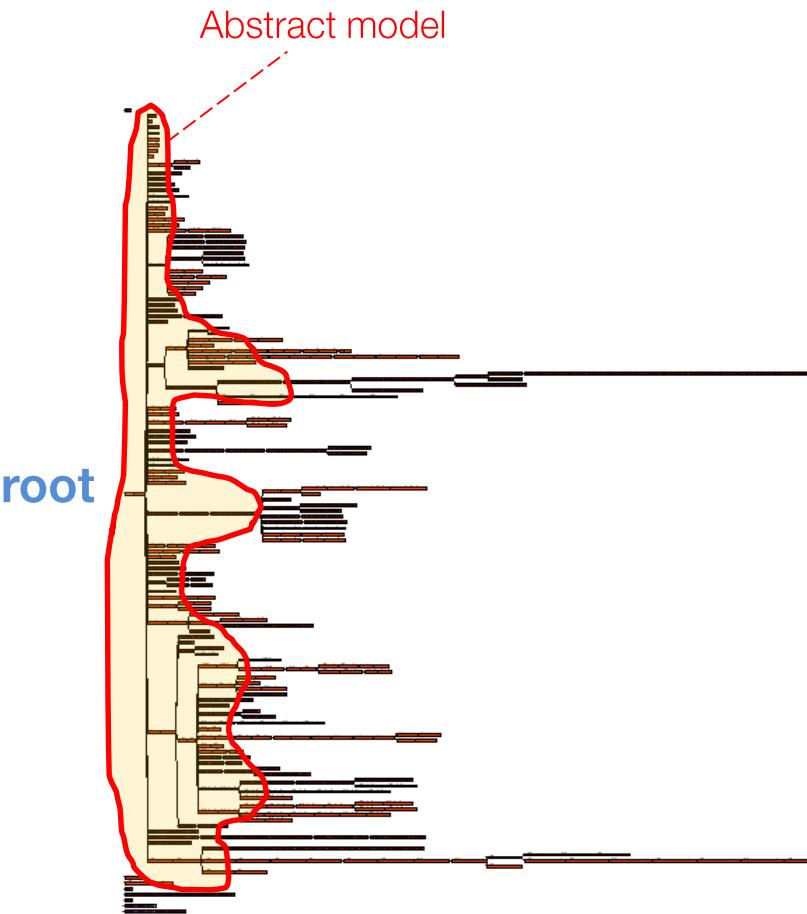
- Project** window: Shows versioned projects "UEVOL (10.2.8)" and "UEVOL (10.2.5)". A red circle highlights the "UEVOL (10.2.5)" section.
- B model + tags (PRAGMAS)** window: Displays B model code with pragmas, including requirements like "Requirement(begin, "CC_ATP-A401464-SwRS-1056-1")". A red circle highlights the code area.
- Requirement CC_ATP-A401464-SwRS-1292-1** window: Provides requirement details, original document ("Document.doc"), body text ("ctrl_MINABIS_counter_end1 = Other CC Synchro Report Minabis Distance Counter for end 1(Cycle)"), and a comment field. A red circle highlights the requirement details.
- Specifications** window: Shows "Specifications" with a table including columns for Specification, Requirements, and Coverage (%). A red circle highlights the coverage table.
- Pragmas** window: Shows the "ctrl_MINABIS_counter_end1 = Other CC Synchro Report Minabis Distance Counter for end 1 (Cycle)" entry.

Annotations in red text:

- B model + tags (PRAGMAS)**: Labels the B model code window.
- Coverage**: Labels the Specifications window's coverage table.
- Requirement**: Labels the requirement body text in the requirement details window.

Automatic Refinement

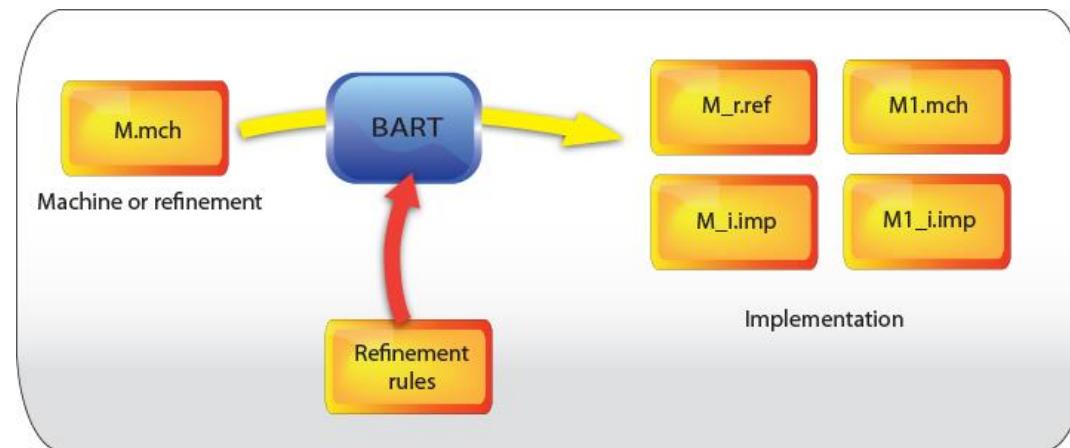
Abstract model



≡ Progressive transformation of a model containing all design decisions into a model able to be translated into an imperative language

≡ Initially invented by Matra Transport

- To support their own development methodology (abstract model first)
- In-house tools (EdithB + Bertille) to obtain an efficient process
- Refinement engine based on refinement rules



Modern Automatic Train Protection Software
(2015)

Automatic Refinement

- ≡ Not a push-button tool
 - Automate what the modeller does manually
 - Refine variables then substitutions
 - Adding rules is mandatory when automatic refinement fails (iterations)
 - Rich language: type information, operation declaration, etc.

```
RULE assign_a_bool_belongs_b_c_16
REFINES
  @a := bool(@b|->@d : @c*@e)
REFINEMENT
  @a := bool(@b:@c & @d:@e)
END;
```

Used rule:

```
RULE r_ens
VARIABLE @a
TYPE
  setarrayNAT(@a)
WHEN
  @a <: NAT
IMPORT_TYPE
  @a <: NAT
CONCRETE_VARIABLES
  @a_i
INVARIANT
  @a_i : NAT --> BOOL &
  @a = @a_i~[{TRUE}]
END
```

Variable to refine:

```
ABSTRACT_VARIABLES
  sub
INVARIANT
  sub <: NAT
```

Refinement result:

```
CONCRETE_VARIABLES
  sub_i
INVARIANT
  sub_i : NAT --> BOOL &
  sub = sub_i~[{TRUE}]
```


Automatic Refinement

≡ No need to certify the tool

- Whatever the refinement rules, in the engine or added by users
- If the refined model is incorrect, it can't be proved

≡ Impact on projects

- Siemens claimed to divide development costs by 2 when the process is stabilized
- More little steps, more decomposition levels, more function calls, more lines of code
- Refinement patterns ease deployment of proof strategies

≡ Industrial applications

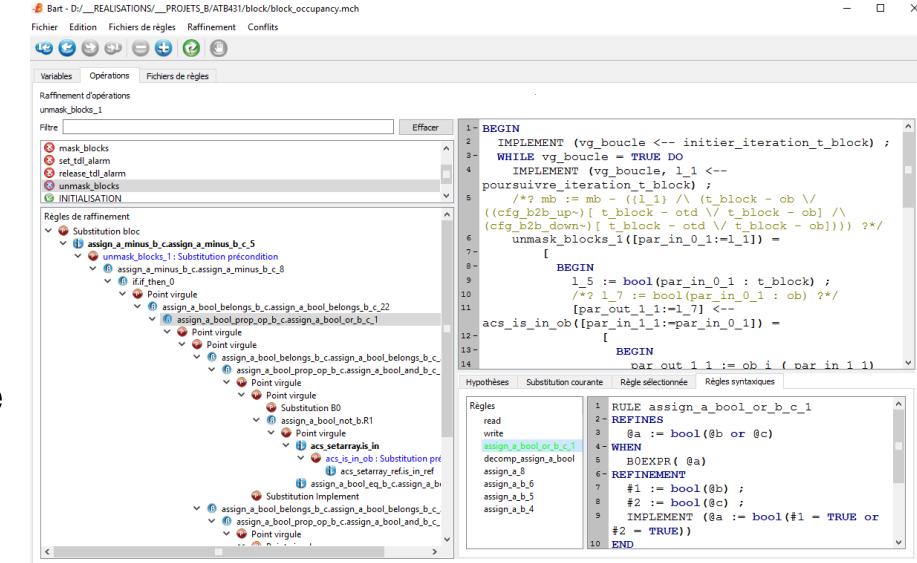
[2004] Canarsie line (ATP):

[2007] Roissy airport shuttle (ATP+ZC):

[2007] Symbolic Calculus Engine:

[2015] SysML Compiler :

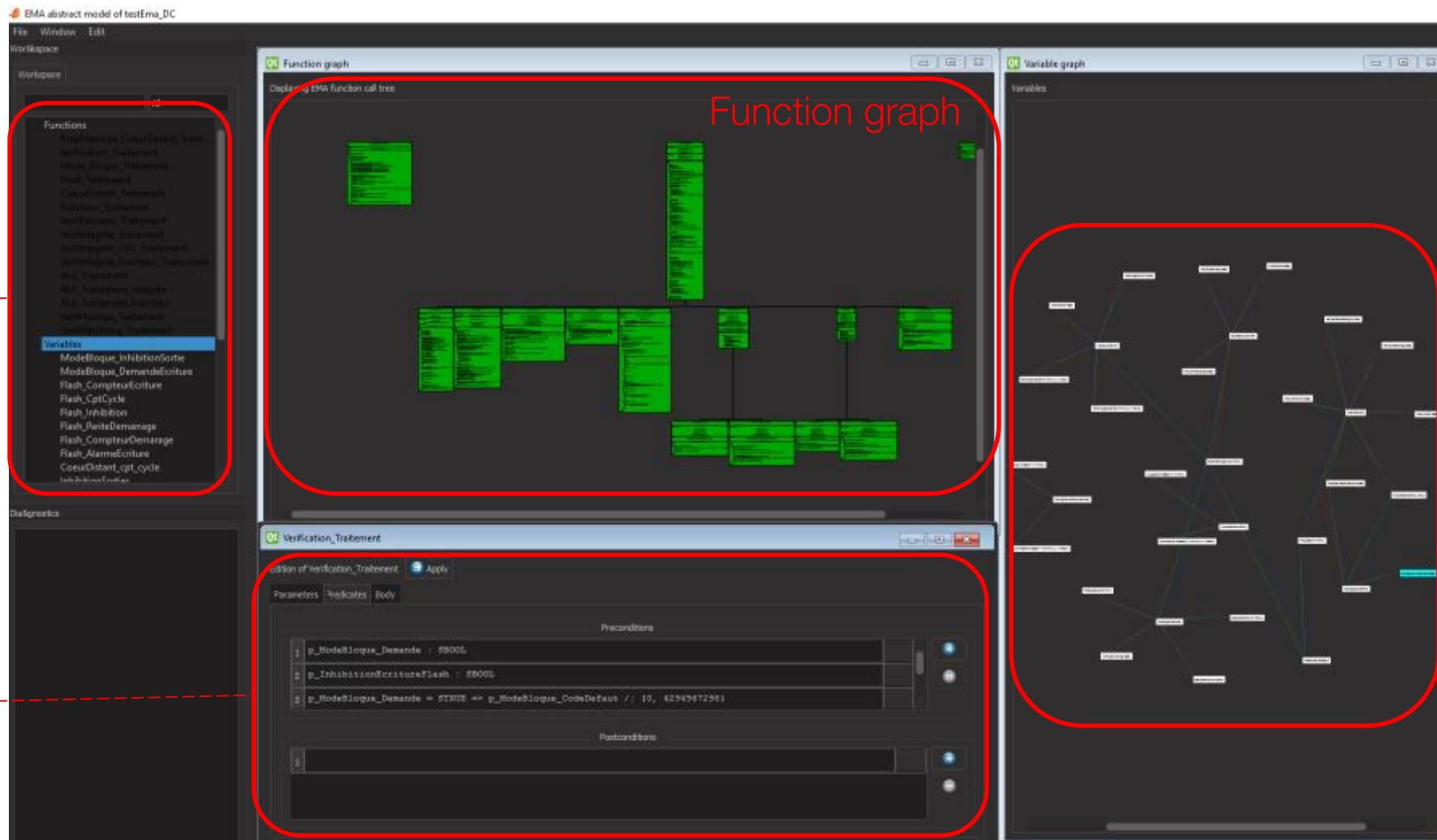
*38k lines of handwritten B,
115k lines of generated B
40k lines of handwritten B
225k lines of generated B
200k lines of generated B
300k lines of generated B*



B Automatic Refinement Tool (BART) added to Atelier B in 2007, in accordance with Siemens T.S.

Simplified Abstract Modelling

- ≡ Propose a new way of modelling
- User is incited to think in terms of functions
- Model creation, decomposition, variables allocation is left to the computer



Outline

- Functions
- Variables
- Constants

Function

- Parameters
- Predicates
- Body

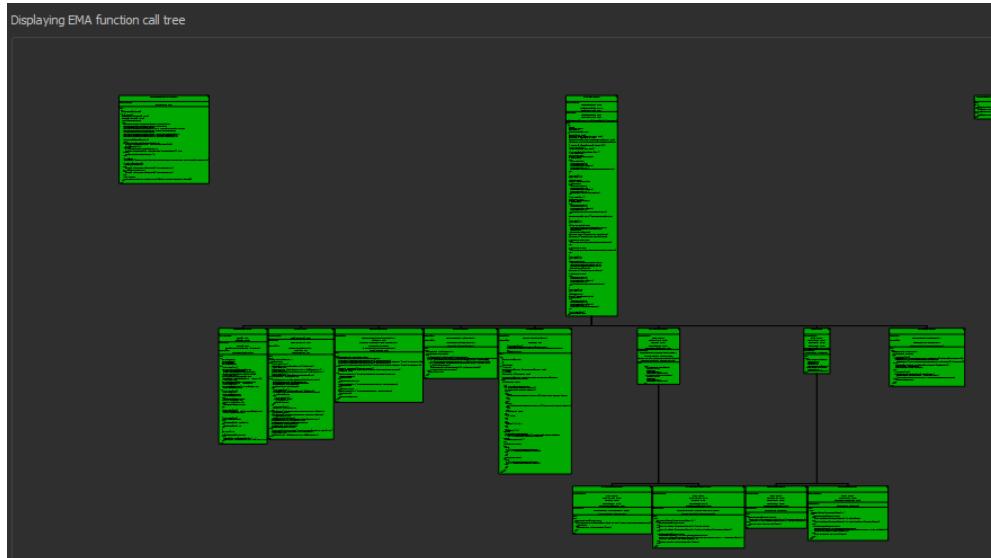
Variables graph

- What is produced
- What is consumed

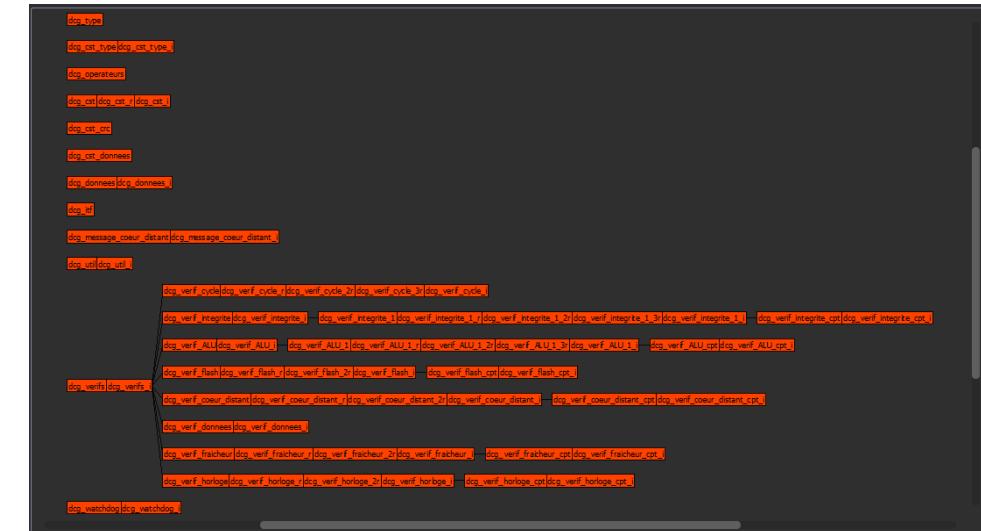
Simplified Abstract Modelling

≡ Two Modelling Views for the Same Project

- Projects can me edited what ever the view
- Providing a clear distinction between abstract model and concrete model
- Corollary: not all projects can be analysed
- Direction continuation of the Automatic Refinement approach



Abstract Modelling Editor (EMA) to appear in Atelier B 4.4

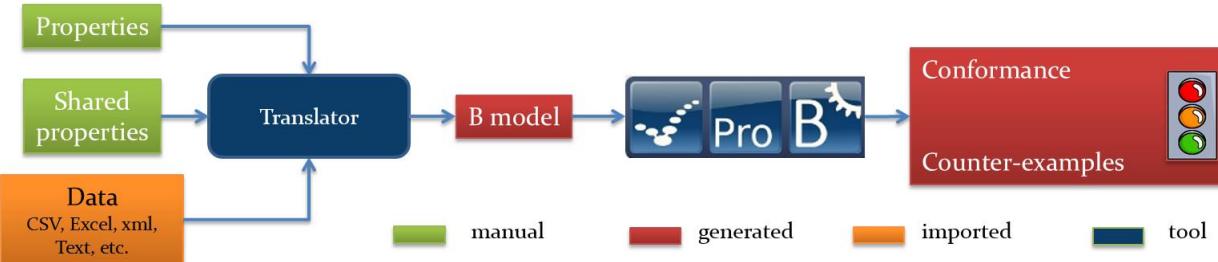


Atelier B current component view

Formal Data Validation

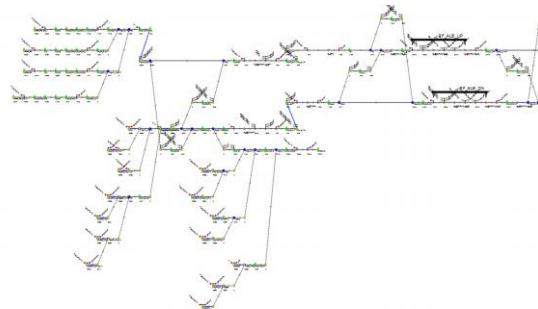
≡ Consistency, correctness, safety

- Expressed with the mathematical language of B
- Work well with graph-based properties
- Provide counter examples when errors found



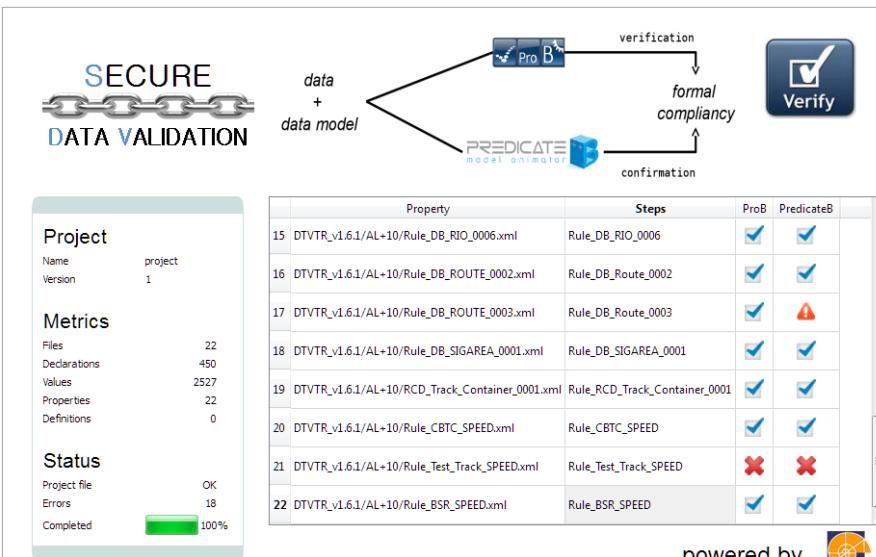
≡ Model-checking

- Performed with ProB
- Rodin (Siemens) and Alstom have funded development and validation to obtain mature tool
- Replace months of (boring) engineer work by hours of computer verification
- Engineer models properties (1 000/line)



≡ Industry-Ready [PUSH-BUTTON !]

- Deal with permanent changes in data and properties
- Redundant tools to obtain diversity
- Rules reused from one project to another
- More than 30 sites verified including:
 - Singapore, Panama, Ryad, Mecca



Formal Data Validation

≡ Example of Properties

- Domain Specific Language to express properties
- Direct translation from the DSL to B
- This rule is simple

FOR

sig, ixl

WHERE

```
sig : sys_sud_er::Signal &
sig : dom(sys_sud_er::Signal_dptId) &
sig : dom(ic::sys_sud_er::signal_geopoint) &
ic::sys_sud_er::signal_geopoint(sig) : ic::sys_sud_er::zone_GPZone (sys_sud_er::IXL_Core_singleZone(ixl))
```

THEN

VERIFY

```
    sys_sud_er::Signal_dptId(sig) : ran(sys_sud_er::IXL_Core_signal(ixl))
```

MESSAGE

«The signal %1 belongs to IXL_Core %2 territory but is not referenced among its signals.»

ARG sys_sud_er::Signal_name(sig) TYPE STRING

ARG sys_sud_er::IXL_Core_name(ixl) TYPE STRING

ENDVERIFY

ENDFOR

Formal Data Validation

≡ Verbosity, implicit made explicit

For each GradientTopology (GradientTopology.BOT-Zone) totally included in a segment, a Gradient (Gradient.BOT-Zone) is created with the same attributes.

For GradientTopology intersecting different segments, several Gradients (Gradient.BOT-Zone) are created so that each of them is located in only one segment.

When the gradient is constant (GradientTopology.isConstant = Yes):

- the variable gradient information (Gradient.VariableGradient) is not set.
- the constant gradient information is set with the same information of GradientTopology for both parts.
- the elevationDifference.elevationEnd of the part1 and elevationDifference.elevationStart of the part2 (reference to the above figure) are equal to elevationStart + gradient*Length1.
- the information isConstant is set to Yes for both parts.

When the gradient is not constant (GradientTopology.isConstant = No):

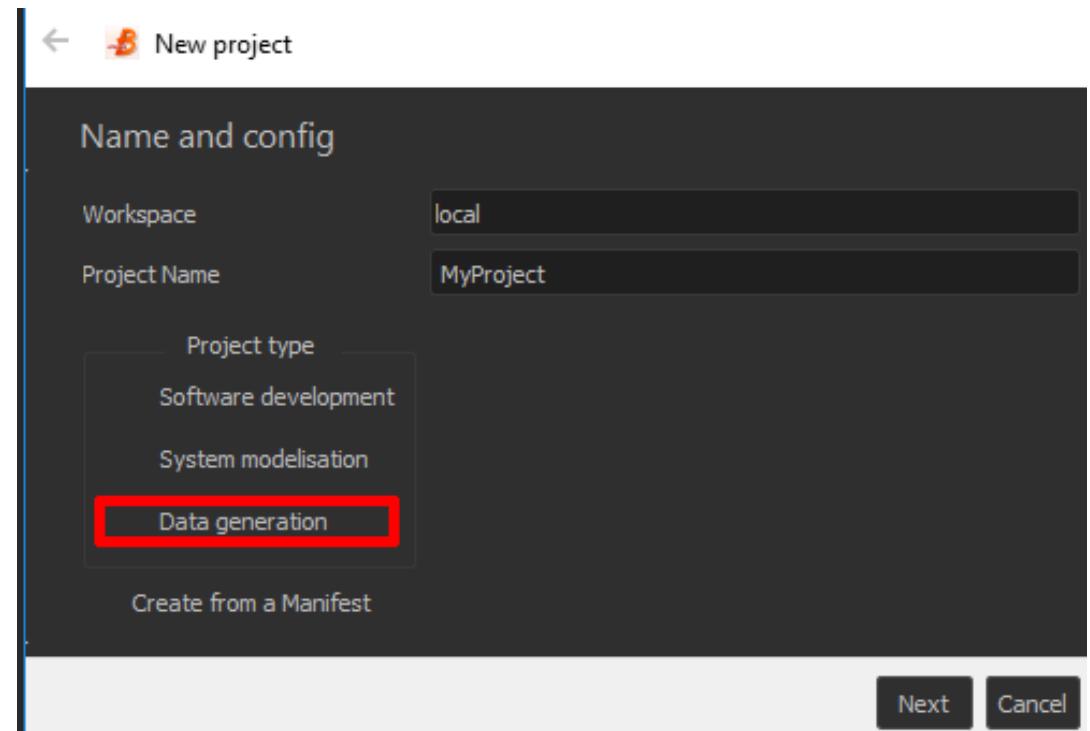
- the constant gradient information (ConstantGradient) is not set.
- the elevationDifference.elevationEnd of the part1 and elevationDifference.elevationStart of the part2 (reference to the above figure) are equal to elevationStart + $2 * \text{radius} * \sin(\text{Length1} / (2 * \text{radius})) * \sin(\text{gradientStart} + \text{Length1} / (2 * \text{radius}))$.
- the information radius and transitionCurveType of the variableGradient information are the same for both parts (as initial GradientTopology information) .
- the information gradientEnd for part1 and gradientStart of part2 for variableGradient information are set to $(\text{gradientEnd} - \text{gradientStart}) / (\text{Length1} + \text{Length2}) * \text{Length1} + \text{gradientStart}$.
- the information isConstant is set to No for both Part.



Formal Data Validation

≡ New feature

- Added to Atelier B 4.2
- Requires ProB to be installed
- Able to validate constants against properties
- Able to generate/compute missing values



Event-B

≡ Involved in Several R&D projects

- French proposal rejected “because Event-B mathematics do not allow to model systems” (*sic*)
- FP5 **MATISSE** (Methodologies And Technologies for Industrial Strength Systems Engineering)
 - First language draft specification
 - Software-based systems
 - Event-B to B translation to experiment
 - UML-B
- FP5 **PUSSEE** (Paradigm Unifying System Specification Environments for Proven Electronic Design)
 - Electronic-based systems
 - VHDL code-generation
- FP6 **RODIN** (Rigorous Open Development Environment for Complex Systems)
- FP7 **DEPLOY** (Industrial deployment of system engineering methods providing high dependability and productivity)

Non Safety Related Applications

≡ Event-B applied to a number of diverse applications

- Banking (Société Générale)
- Ariane 5 Flight Sequencer Software (Délégation Générale de l'Armement) ----- "When we fire a nuclear missile underwater, we want to be sure that the 'door' is open"
- Micro-Satellites Constellation Flight (Centre National d'Etudes Spatiales)
- Air Traffic Control (Eurocontrol, CEAT) ----- "An Air-France flight landed in Brussels with guidance from Zurich airport"
- Press (Caisse Nationale d'Assurance Maladie)
- De-icing Helicopters (Eurocopter)
- Nuclear Plant (Electricité de France) ----- "Trust me: you don't want to know"
- Multiplexed Cars (Peugeot, Renault)
- Smartcard (STMicroelectronics)
- Etc.

≡ No positive conclusion

- understanding,
- compliance with existing development cycle & methods,
- existing teams,
- standards,
- etc.

≡ Except

- Vehicles (diagnosis, assistance to integration)
- Smartcard (certification, proven product)
- Railways (safety critical systems)

Component-Based System Description

≡ Flat Behavioural Specification (maintenance, failure diagnosis)

- Event-B to describe behaviour, light proof
- Find ambiguities in the specification documents (thousands pages)
- Events are allocated to components
- Analyse model structure to deduce dependencies: where is produced, where is consumed
- Generate documentation from model and additional information

B model

```
F_Opening =
SELECT
    CommandOpening = TRUE
THEN
    PSDOpen := TRUE
END;
```

Dictionary

```
VARIABLE PSDOpen
MEDIUM Internal
TRANSLATION
    Status of the non locked PSD: open or not
END

TRANSLATION PSDOpen:=TRUE
    PSD are opening
END
```

3. Calculateur de quai considéré avec son télémètre (CQx)

COPPILOT est formé des deux calculateurs de quai CQ1 et CQ2, des télemètres TL1 et TL2, de la logique à relais qui fabrique les commandes finales d'ouverture et de fermeture, ainsi que des alimentations et des armatures nécessaires. Ici nous définissons le comportement attendu d'un sous ensemble CQ + TL + alimentations nécessaires.

Lois établies sur les paramètres

- loi JamaleCommandeSansTrainCq : si il n'y a pas de train positionné (côté considéré), aucune commande d'ouverture n'est émise par le CQx.
- loi ExclusionFermetureOuvertureCq : Les CQ sont faits de telle manière qu'ils ne commandent jamais en même temps l'ouverture et la fermeture.
- loi PasDeMirePasDeTrainCq : le CQ doit quitter l'état train positionné s'il ne reçoit plus la mire.
- loi ApresOuvertureSiOuvertureCq : Si une commande d'ouverture est active, alors le CQ doit mémoriser qu'on est après une ouverture.
- loi PasApresOuvertureSiFermeture : Si une commande de fermeture est active, alors le CQ doit mémoriser qu'on est plus après une ouverture.

3.1.1 Synoptique :



3.2 Paramètres lus

3.2.1 Contact de travail du CDV de quai remonté au CQ



Les événements qui dépendent de ce paramètre sont:

- CQx : Événement dans des situations où CQx ne doit rien faire .
- CQx : Détection d'un train alors que le CDV est libre .

Les événements au cours de lesquels ce paramètre évolue sont:

≡ Modelling Main Issue

- What could be done when millions hours have been spent designing a car ?

Component-Based System Description

≡ Tooling

- Scripts developed during modelling sessions turned into a standalone tool: Composys
- Based on Atelier B BCompiler

Killed In Action 2012

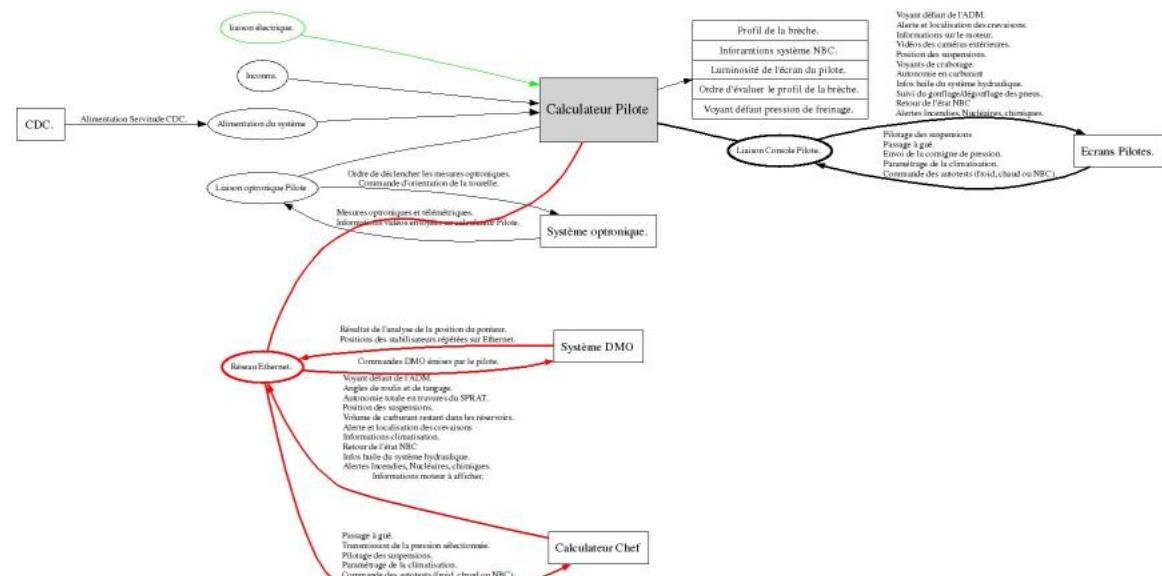
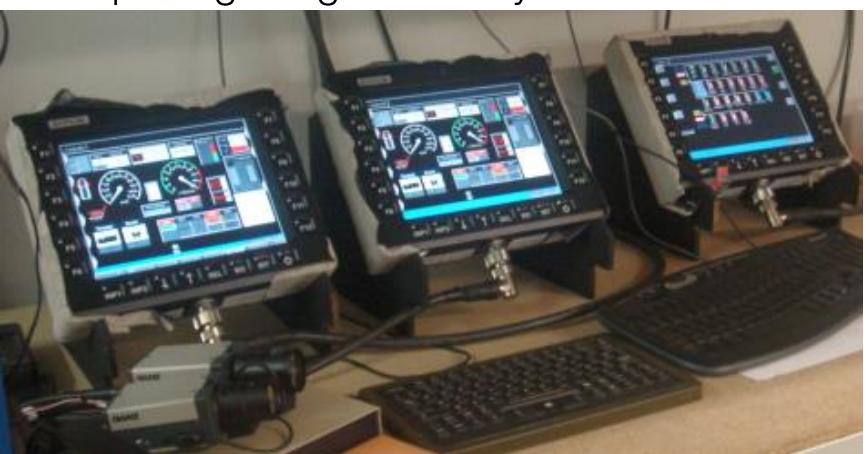
≡ Cars Modeling

- Applied to the failure modelling of 4 Peugeot cars in order to locate faulty ECU(s)
- To help mechanics to diagnose failures
- Stopped in 2005, Peugeot switched back to only provide error codes without further analysis

```
Reponse_ID =  
SELECT  
    vl_coupleage = normal &  
    Attente_reponse = TRUE &  
    PresenceIDCoteDroit = TRUE  
THEN  
    ID_Reponse :: {REP_pirate, REP_PSA} ||  
    vl_coupleage := ph_Emission_reception  
END
```

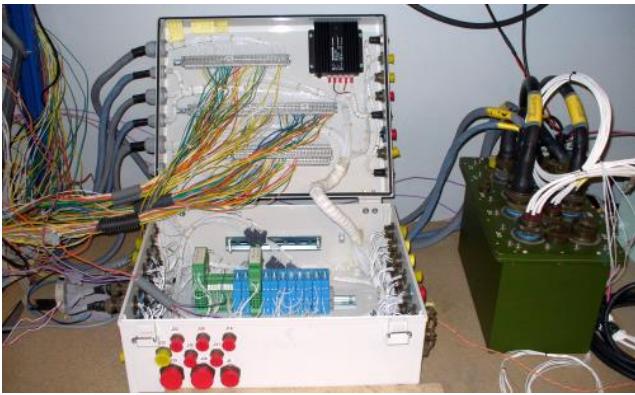
≡ Military Vehicle Modeling

- Applied to the design of unique vehicle designed from scratch
- To help integrating tons of systems



Component-Based System Description

= On Going Integration

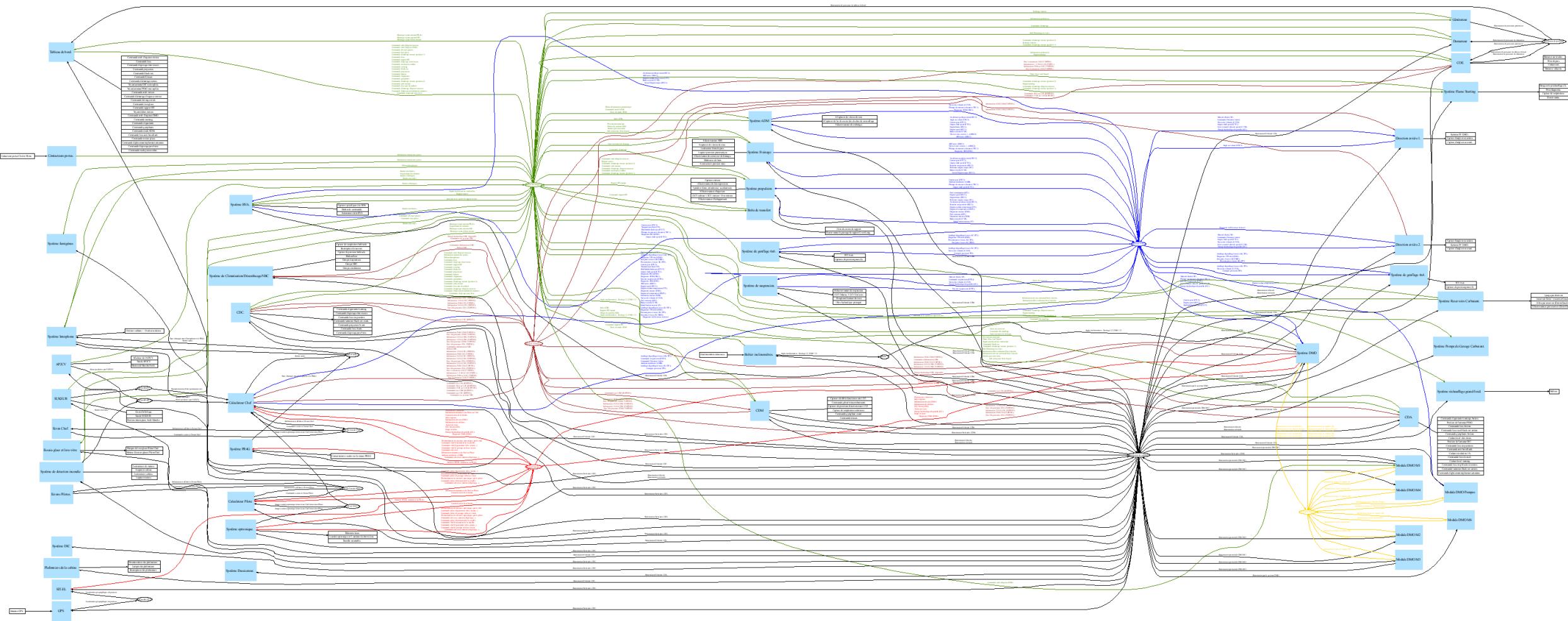


= The Resulting Vehicle



Component-Based System Description

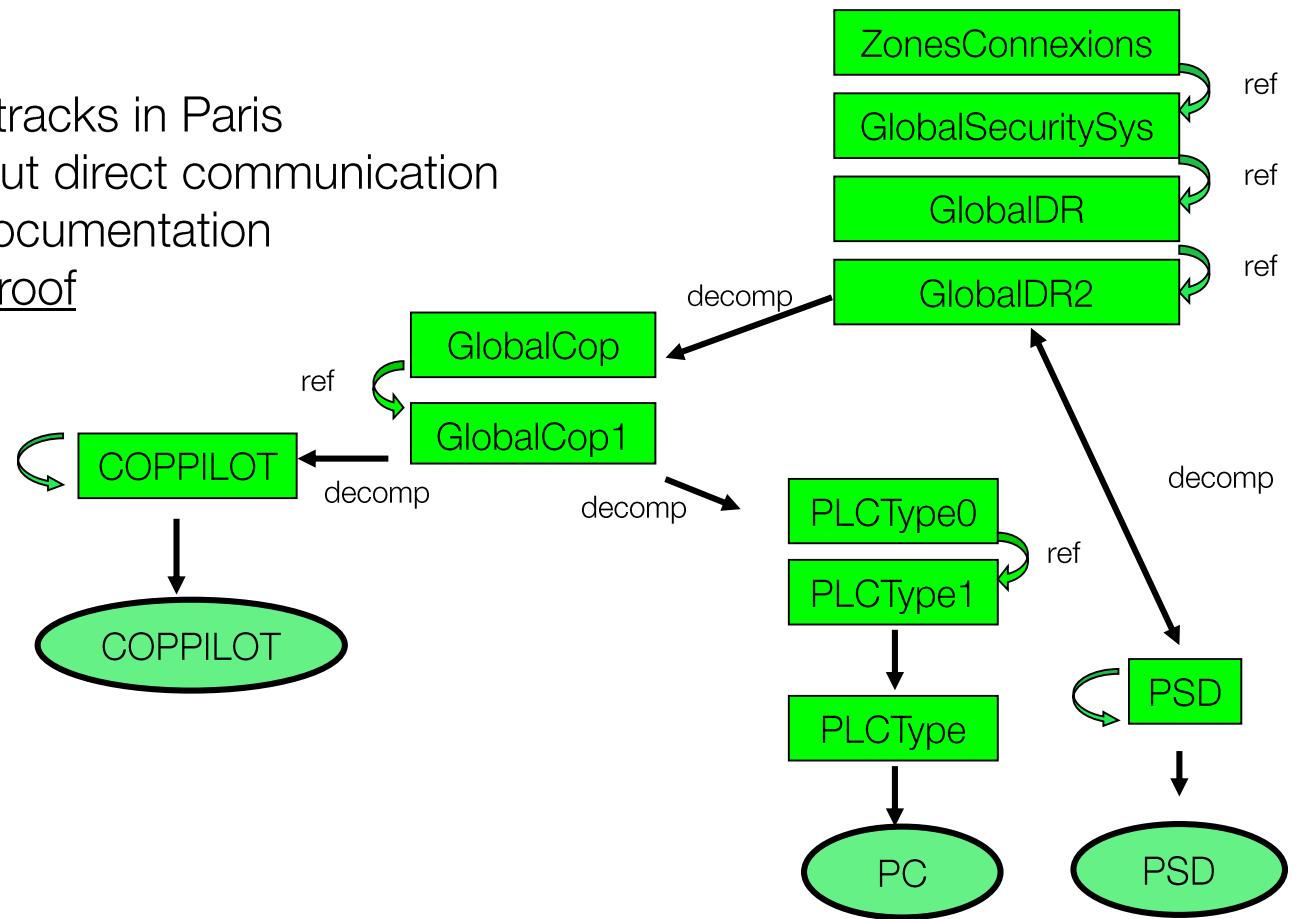
≡ Complex Relationships



Component-Based System Description

≡ Platform Screen Doors (railways)

- New system to avoid people to die (pushed) on tracks in Paris
- Trick: detect train arrival and door opening without direct communication
- Composys to analyse the system and provide documentation
- Finally an Event-B model to ensure safety with proof



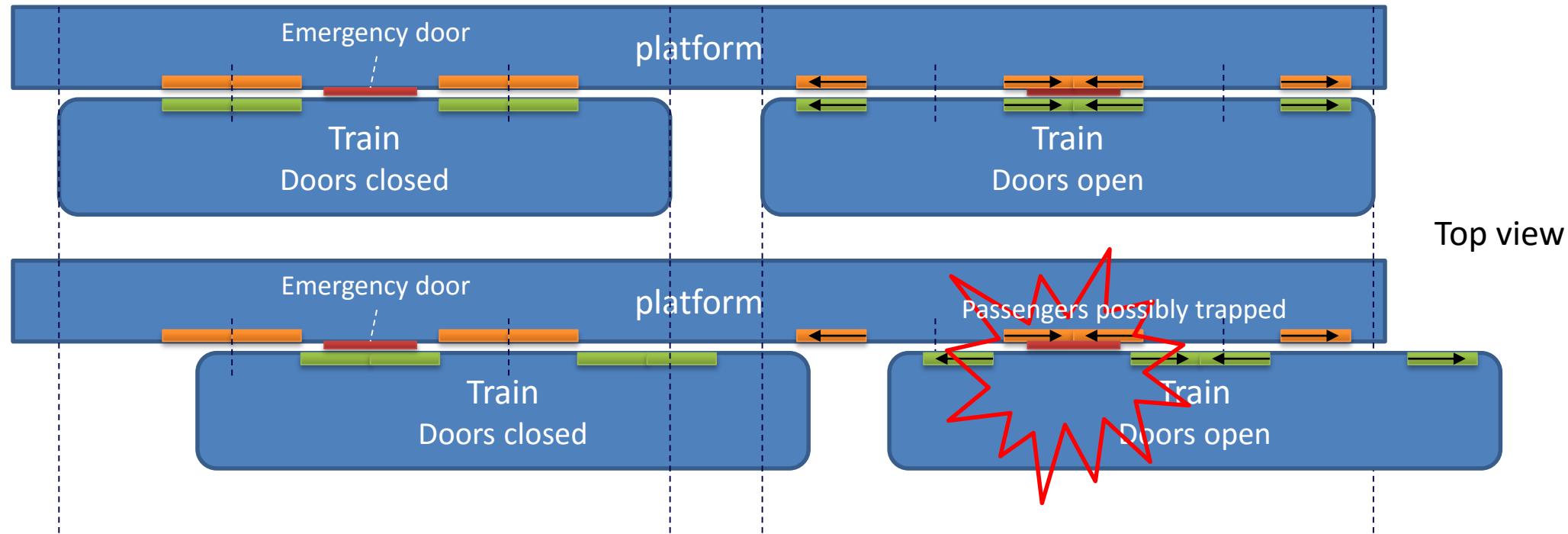
≡ Real System on Paris L13 (proof of concept)

- Developed from scratch in 6 months
- Lot of missing skills to acquire
- Software developed manually from formal specification
- SIL4: one failure every 10 000 years
- 99,999% reliability: one train max missed per year
- one year successful experiment: no death, no train missed

Component-Based System Description

≡ Proved but still unsafe ...

- Proven Event-B model presented to RATP
- But major issue uncovered by RATP technician



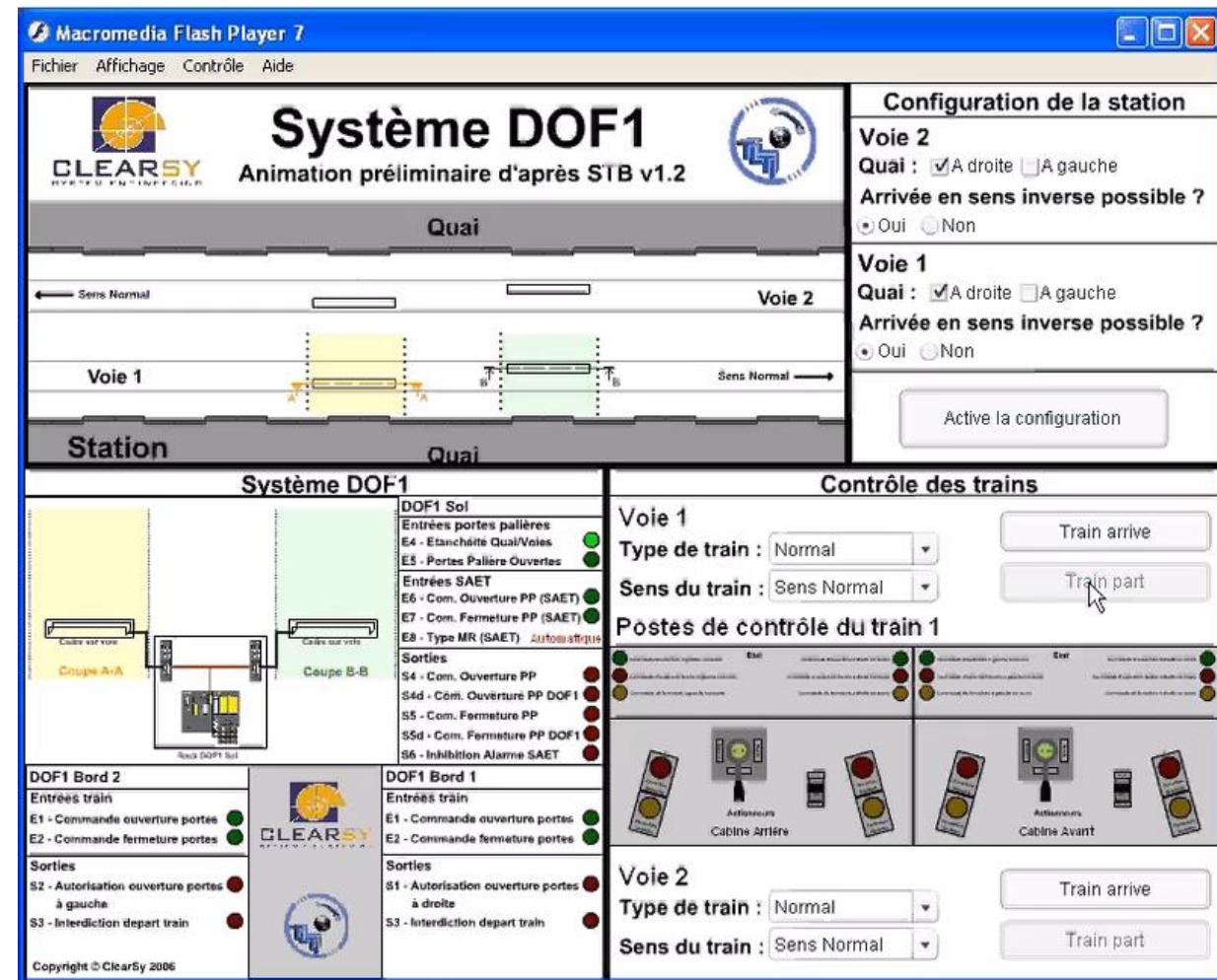
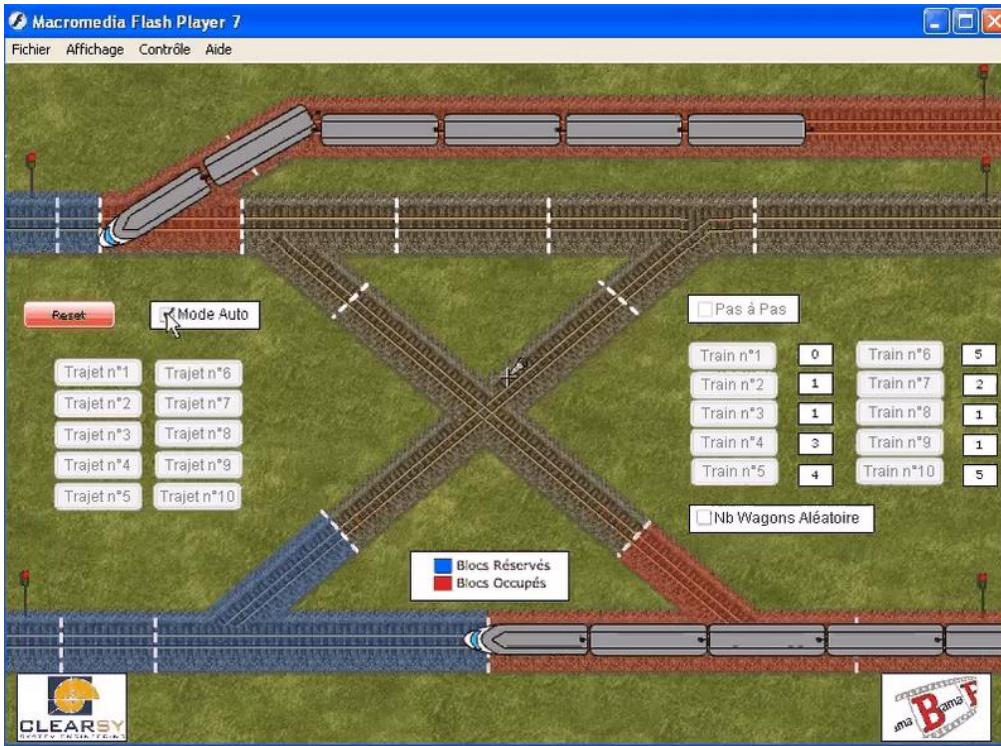
≡ Specification changed: “do not open PSD in case of incorrect train position”

- Did we select the “correct” dimensions to analyse the system ?
- What about Japanese tourists taking pictures on the other platform, birds flying through the tunnels, etc. ?

The model

≡ For the next call for tender (Paris line 1), we were ready

≡ Brama Model Animator (Rodin)

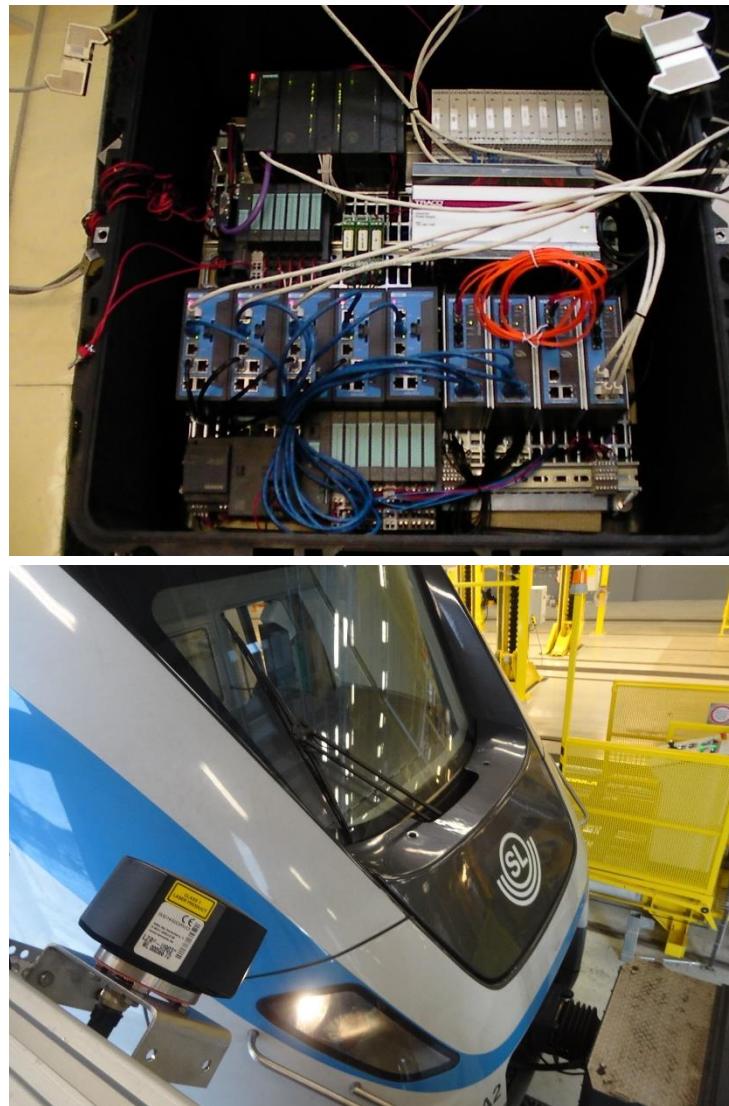


The model

≡ When it is the first time, it is the first time !



Scale 1 DIY model



The model

≡ Connecting things with the real station



Et voilà !

Security & Common Criteria

≡ Smartcard industry demands for higher security levels

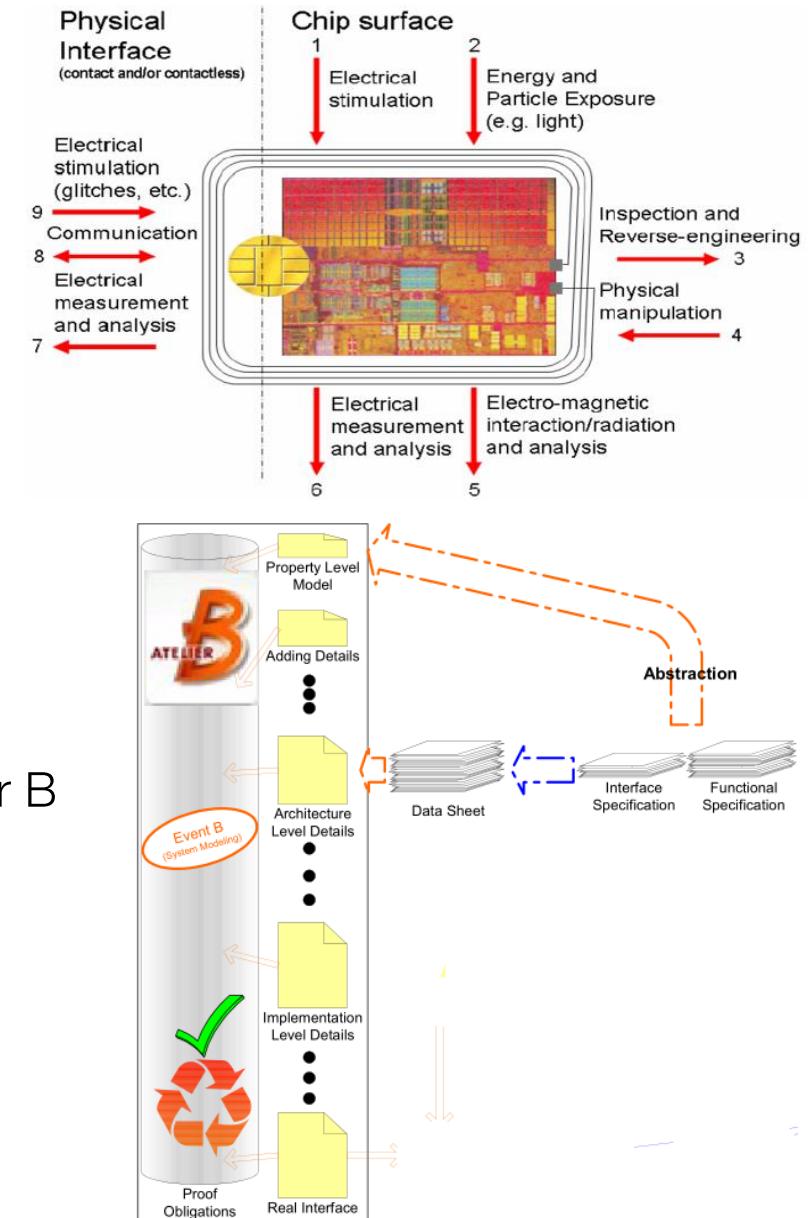
- ... for marketing reasons
- First attempt:
 - Model API functions (library available to third-party)
 - Model Security Policy (define what access conditions are)
 - Prove that Security Policy is enforced by the functional specification
 - Check (traceability) that specification is implemented
 - Compliant with EAL5+ (Common Criteria 2.2)
 - 1 Event-B model, 4 levels of refinement
- Replayed several times for different companies and products
- Demonstration is limited to non-disturbed behaviour *"When it works, it works"*

≡ Down to the hardware

- Same approach than above, *Rodin not op*, Event-B support added to Atelier B
- Component to study: Memory Protection Unit
- 1 Event-B model, **18 levels of refinement**, ready for VHDL code generation
- Development: 6 months, 183 versions, 5 major refactoring
- Final product: **20 000 gates**

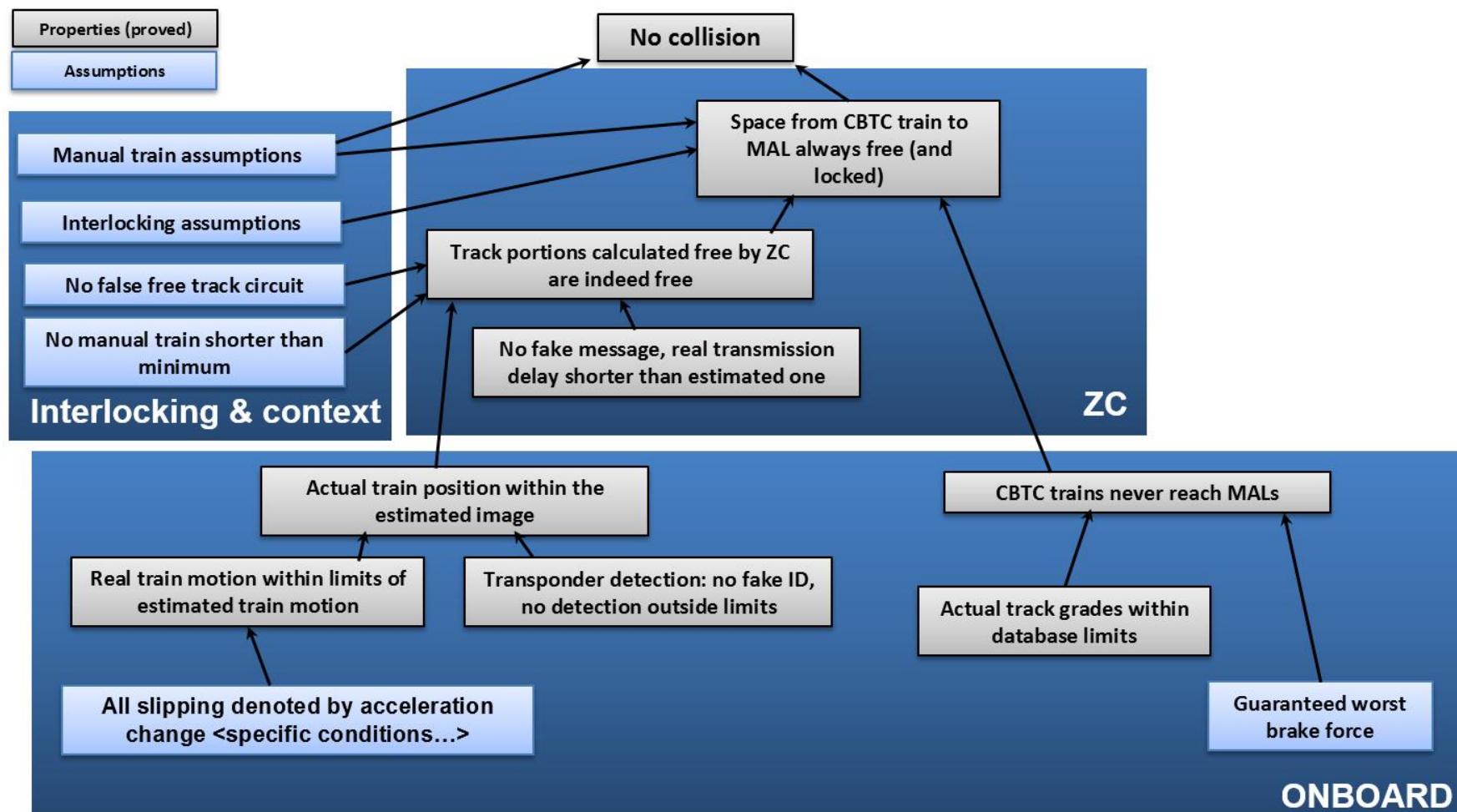
18 levels for an IF-THEN-ELSE ???

How many levels for Intel Core i7 ?



Safety Demonstration

- 18 levels of refinement for a 20k gates micro-electronic component
- How many zillions levels required to model a metro line **and** address very low level details ?
- Challenge: proving that a new CBTC (Thales) enforces safety on New York L7 metro
 - No structural “model of everything”
 - End-product readable and understandable by customers
 - Reusable on other lines

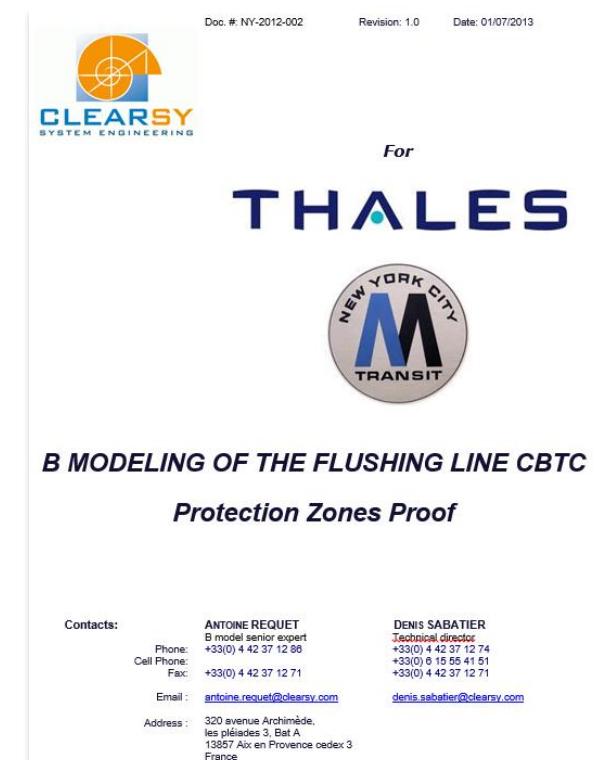
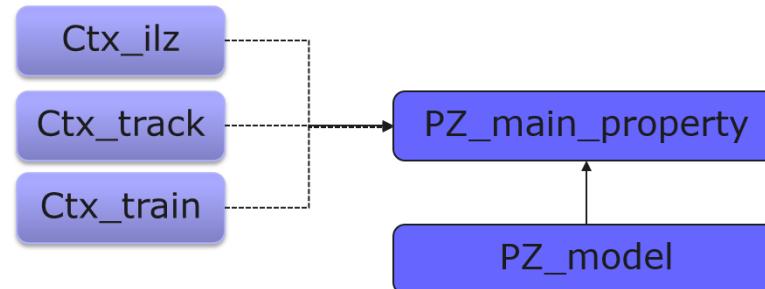


Safety Demonstration

- Protection zone proof: 35 assumptions, 2 subproofs, 30 events, 1400 loc model
- 2 years to complete
- NYCT analysed positively the proof documents
- Reused on Culver line (50% effort reduction)
- Experimented on:
 - ERTMS Regional
 - Paris metro (xx lines automated until 2030)

Reference:

D. Sabatier, L. Burdy,
New York Metro Flushing line: System level formal verification ,
June 2013



Proof document: 90 pages

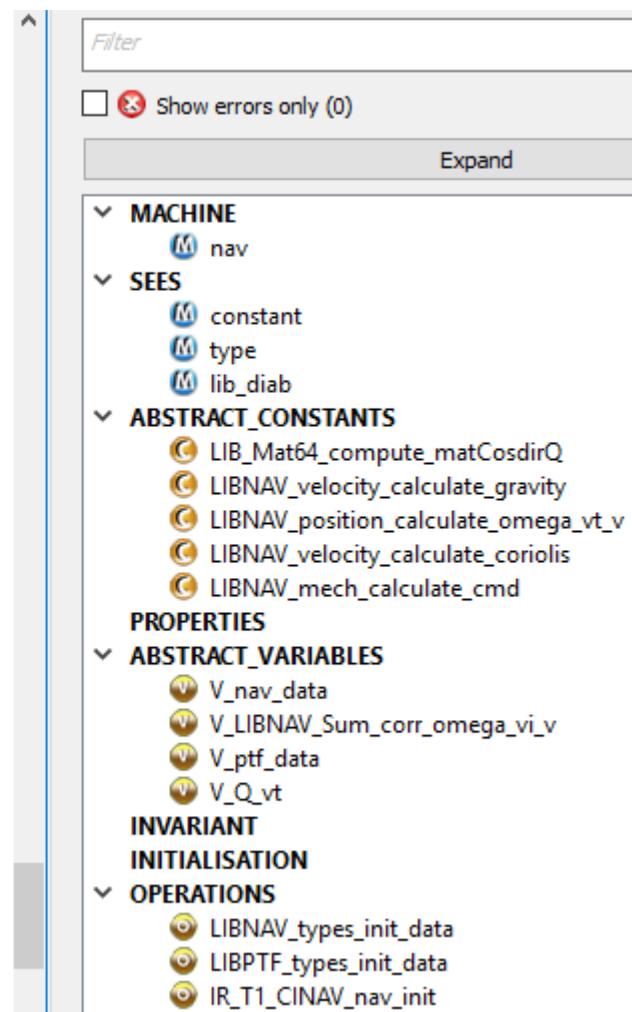
Real & Floating Point Numbers

≡ New proof obligations

- Not currently handled by any prover
- Bware project would contribute to it

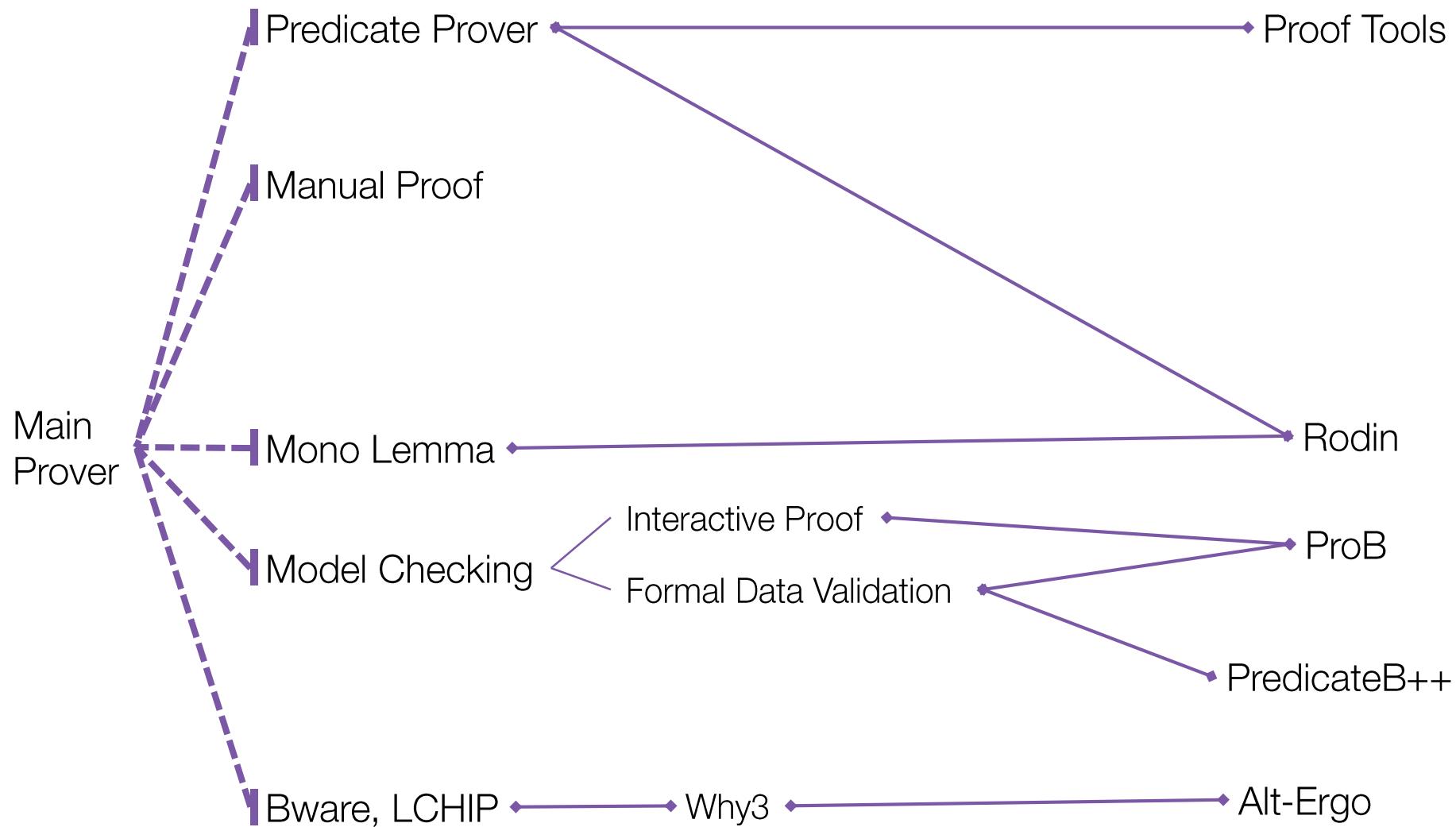
```
LIBPTF_types_init_data =
BEGIN
    /* Init pure inertial attitudes */
    V_ptf_data := rec ( pure_inertial_attitudes : rec ( Roll : 0.0 ,
Pitch : 0.0 , Azimuth : 0.0 ) ,
T_vm : % xx . ( xx : 0 .. 2 | ( 0 .. 2 ) * { 0.0 } ) ,
T_vb : % xx . ( xx : 0 .. 2 | ( 0 .. 2 ) * { 0.0 } ) ,
deltaV_v : ( 0 .. 2 ) * { 0.0 } ,
q_vm : ( 0 .. 3 ) * { 0.0 } )
END ;

IR_T1_CINAV_nav_init ( p_Velocity_InitVALUE , p_Position_InitVALUE ,
v_vertical_velocity , v_altitude , v_deltaT ) =
PRE
    v_deltaT : tFloat32 &
    p_Velocity_InitVALUE : tVect3_64 &
    p_Position_InitVALUE : tVect3_64 &
    v_altitude : tFloat64 &
    v_vertical_velocity : tFloat64
THEN
    LET
        pa_coriolis_correction ,
        v_vect_pos_init
    BE
        /*! Init Velocity */
        pa_coriolis_correction = ( 0 .. 2 ) * { 0.00 } &
        v_vect_pos_init = ( 0 .. 2 ) * { 0.00 }
    IN
```



Proving

Proving



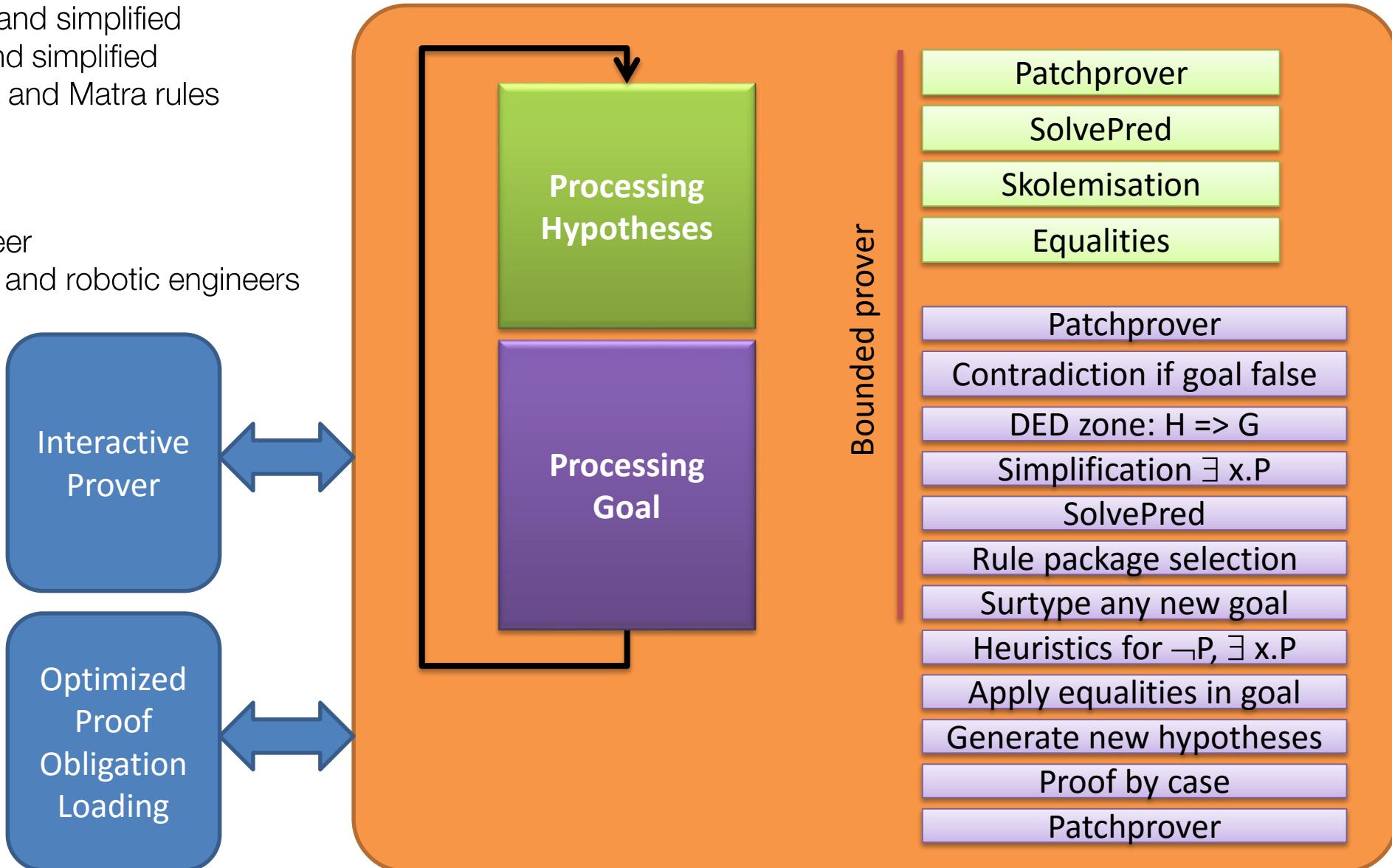
Main Prover

≡ Rule-based Proof Engine

- Predicates are decomposed and simplified
- Hypotheses are generated and simplified
- Set of rules includes Alsthom and Matra rules

≡ State of the Art

- Invented by a signalling engineer
- Improved by electrotechnician and robotic engineers



Main Prover

≡ Ad-hoc programming language: THEORY language

- Prolog-like
- Built-in B parsers
- Programs transformed in bytecode programs executed by a VM
- Integrated to Rodin as a plugin (Mono Lemma version)

```
IDENT(InRelationXY.11)
binhyp(r: s <-> t) &
binhyp(q: s <-> t)
=>
(r/\q: s <-> t);
```

Leaf rule

```
IDENT(InRelationXY.7)
(dom(b)<<|a: s <-> t) &
(b: s <-> t)
=>
(a<+b: s <-> t);
```

Equivalence rule

≡ Fixed point

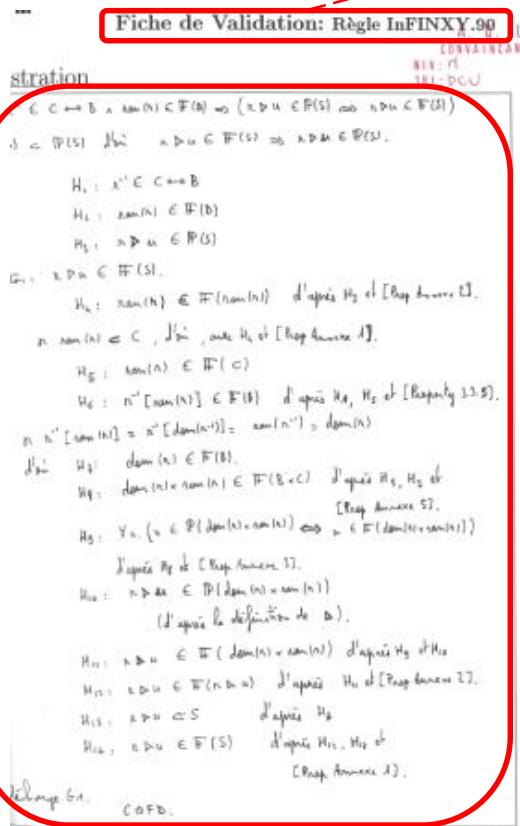
- 1 proof obligation to demonstrate manually == 35 €
- No proof regression allowed with atelier B releases
- Since 1998, evolutions are new interactive commands and triggerable sets of rules

```
THEORY SimplifyDisjX IS
  bcall(WRITE: bwritef("Impossible
=>
p;
SimplifyDisjG(A | a | R);
bcall(RES: bresult(R))
=>
SimplifyDisjG(a | a | R);
bsearch(a, (A or bfalse), B) &
bcall(RES: bresult(R or B))
=>
SimplifyDisjG(A | a | R);
SimplifyDisjG(A | a | R)
=>
SimplifyDisjG(A or a | a | R);
bsearch(a, (B or bfalse), C) &
SimplifyDisjG(A | a | R or C)
=>
SimplifyDisjG(A or B | a | R);
END
```

Main Prover

≡ 2 700 rules to validate

- Manual demonstrations
- Cross-verification
- Third-party verification



Manual demonstration

```

hyp2 f~; s ~> NATURAL
hyp3 e; s
hyp4 note(e; ran(f))
but (f~e)~; s ~> NATURAL

hyp5 f~e = f~/(size(f)+1)->e)~; s ~> NATURAL          DR11 sur L (Hyp1 Hyp3)
      <- f~/(size(f)+1)->e)~; s ~> NATURAL      Inverse Properties
      <- f~/(e~>size(f)+1); s ~> NATURAL      Inverse Properties
      1.1 <- f~; s ~> NATURAL                      Membership Properties
      1.2 & (e~>size(f)+1); s ~> NATURAL
      1.3 & dom(e~>size(f)+1)<|f~ = dom(f~)<|(e~>size(f)+1)

1.1   décharge par Hyp2
1.2   décharge par Hyp3

1.3   dom(e~>size(f)+1))<|f~           Domain Properties
      = (e~>f~)~                                Inverse Properties
      = (f~e)~                                    Restriction Properties et Hyp4
      = {}                                         Inverse Properties
      = ran(f)<|(e~>size(f)+1))                  ran(f) \ (e) = {} (Hyp4)
      = dom(f~)<|(e~>size(f)+1))                Domain Properties
1.1, 1.2 et 1.3 déchargent le but.

2) On applique DED:
hyp2 (f~e)~; s ~> NATURAL
2.1 f~; s ~> NATURAL
2.2 e; s
2.3 note(e; ran(f))

hyp3 e; s                                     type-checking de Hyp2
hyp4 f~e = f~/(size(f)+1)->e)~              DR11 sur L (Hyp1 Hyp3)
hyp5 f~/(size(f)+1)->e)~; s ~> NATURAL EQL1 sur Hyp2 avec Hyp4
hyp6 f~/(size(f)+1)->e)~; s ~> NATURAL      Inverse Properties
hyp7 f~/(e~>size(f)+1); s ~> NATURAL      Inverse Properties
      par contradiction avec Hyp7
hyp8 f~; s ~> NATURAL

2.1   décharge par Hyp8
2.2   décharge par Hyp3
2.3   par contradiction (Rule 5), on suppose e: ran(f) et on montre:

```

A detailed demonstration

évident (*)
JRA

A concise one !

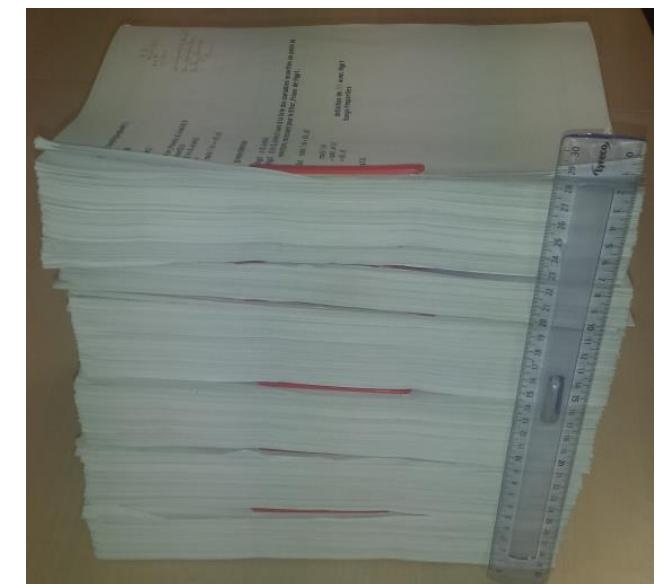
(*) « Obvious »

Testimony:

a rule modified 9 times by 2 experts
while being constantly wrong

≡ The resulting validation forms

- 28 cm



Predicate Prover

≡ Tableau method

- Invented by JR Abrial to prove Atelier B rules
- Used to validate the majority of the 2700 rules of the Main Prover
- Became an interactive command with means to select reduced set of hypotheses
- Integrated to Rodin as a Plugin

```
/** BOOL31 */
INFRULE(BOOL31)
((v = FALSE) => Q)
=>
(not(v = TRUE) => Q);
```

```
/** ECTR6 */
INFRULE(ECTR6)
binhyp(l=m) &
bnot(bgoal(not(L)=>M)) &
bnot(bgoal(!x.H=>N)) &
band(binhyp(F=E),
band(bsubfrm(E,F,P,R),
binhyp(not(R)))
))
=>
(P => Q);
```

≡ Tableau method

- Hypotheses combined with not(goal) to obtain a contradiction
- Heuristics for wise instantiation
- Limited number of rules (116)
- Efficient when the number of hypotheses is low

≡ Added value

- Quickly identify errors

Interactive Proof

≡ Interactive Automatic Proof or Automatic Interactive Proof

- Remember: 1 PO == 35 €
- Improve demonstrations efficiency
 - Abstract and reuse demonstrations
 - Fine grained tactics
 - Motto: do not lose any proof work

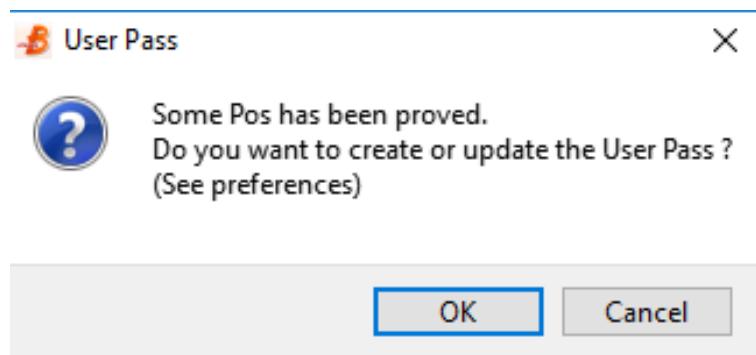


Operation(AssertionLemmas) & Pattern(ST_7 <: E) & dd & ah(Mhyp(ST_7: F)) &p0

Operation filter

Goal filter

Interactive commands



Do not lose any proof work

UserPass creation

preview

```
1 Operation(control) & Pattern(bool(a : {b}\/{c}\/{d}) =  
  bool(bool(bool(a = b) = a or bool(a = c) = a) = a or  
  bool(a = d) = a))  
2   & ff(0) & dd & ah(e0 = e0$1) & ss & pp(rt.1)
```

Generated tactic from successful proof

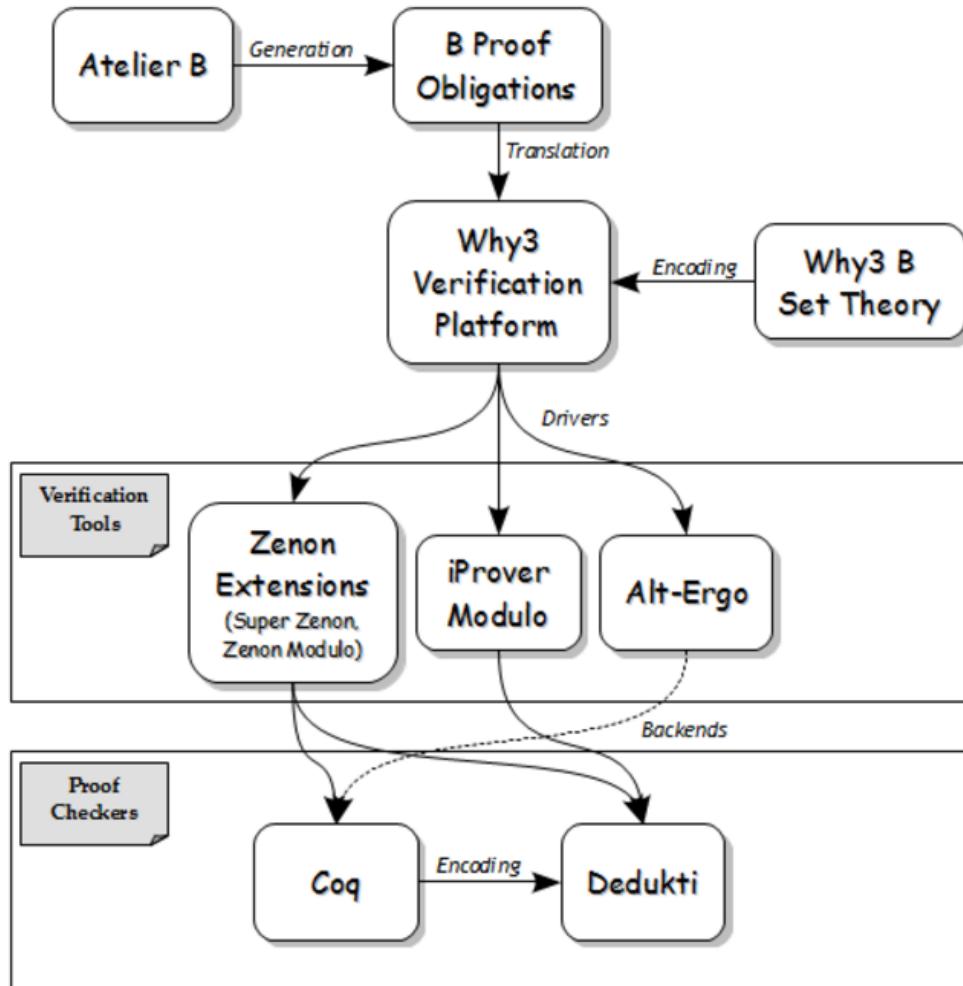
Connecting New Provers

≡ ProB

- Added to Atelier B 4.3.1 as an interactive command.
 - Syntax: prob(n) or prob(n | T).
 - T: timer in seconds,
 - n=1 selects all hypotheses that have a symbol in common with the goal
 - Add resource: ATB*PR*ProB_Path:C:\<path>\probcli.exe
- Funded by Alstom

≡ Alternate provers

- Bware research project (<http://bware.lri.fr/>)
- Connected through Why3
- +100 k Proof obligations (obfuscated) for benchmark
- 78% -> 99% automatic proof for one significant project



Connecting New Provers

The screenshot shows a software interface with a navigation bar at the top: project, software development, krt, resource. The 'software development' tab is active. On the left, there's a sidebar with sections: Type Checker, Proof Obligation Generator, and POG NG. In the Type Checker section, 'Enable extended SEES' is unchecked. In the Proof Obligation Generator section, 'Legacy (<4.2)' is unchecked and 'New Generation' is checked. In the POG NG section, 'Generate Overflow Proof Obligations' is unchecked, 'Generate Well Definedness Proof Obligations' is checked, and 'Generate Why3 Proof Obligations' is checked and highlighted with a red border.

```
goal g_0 :  
forall obf_1: set int, obf_2: set int, obf_3: set int, obf_4: (set int), obf_5: int, obf_6: (set int),  
obf_7: int, obf_8: (set int), obf_9: int, obf_10: (set (int,int)), obf_11: (set (int,int)), obf_12: (  
set (int,int)), obf_13: (set (int,int)), obf_14: (set (int,int)), obf_15: (set (int,int)), obf_23: (  
set int), obf_25: (set int), obf_26: (set int), obf_16: (set int), obf_17: (set int), obf_18: (set int)  
, obf_19: (set int), obf_20: (set int), obf_21: bool.  
(define1 ) /\ (define2 obf_1 obf_2 obf_3 obf_4 obf_5 obf_6 obf_7 obf_8 obf_9 obf_10 obf_11 obf_12  
obf_13 obf_14 obf_15 ) /\ (define6 ) /\ (define7 ) /\ (define9 ) /\ (define10 ) /\ (define11 obf_23  
obf_4 obf_25 obf_26 ) /\ (define3 obf_16 obf_4 obf_17 obf_6 obf_18 obf_8 obf_19 obf_20 obf_21 ) /\ (  
lh_2_0 )  
->  
true /\  
((lh_2_1 obf_4 ) -> (exists obf_27: (set int).(mem obf_27 (power obf_4))))
```

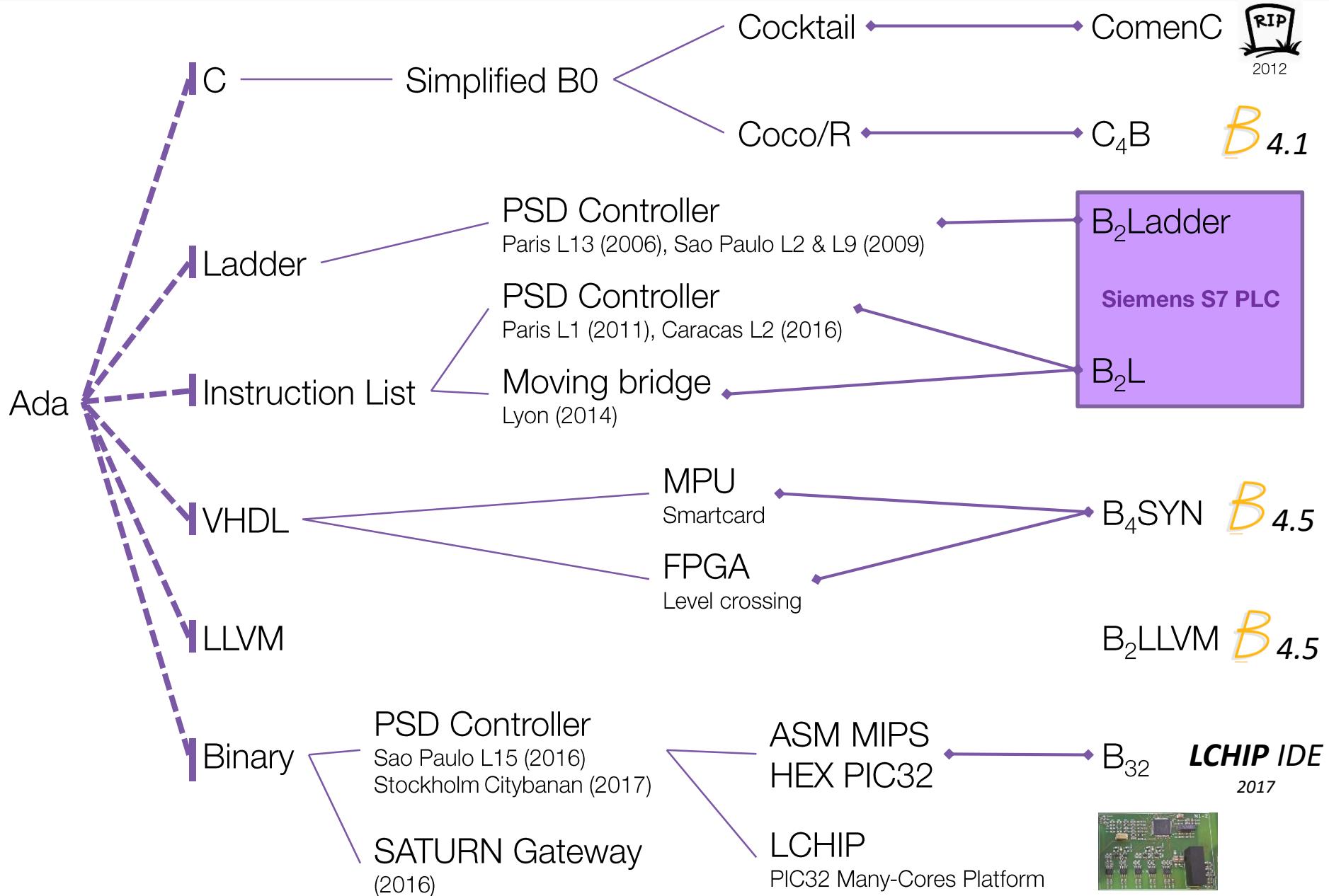
Example of Why3 fragment

≡ Alternate provers (bis)

- LCHIP research project (to start in Q4 2016)
- Connected through Why3, still
- Alt-Ergo integrated to Atelier B, Cubicle model-checker for evaluation

Generating

Generating Code



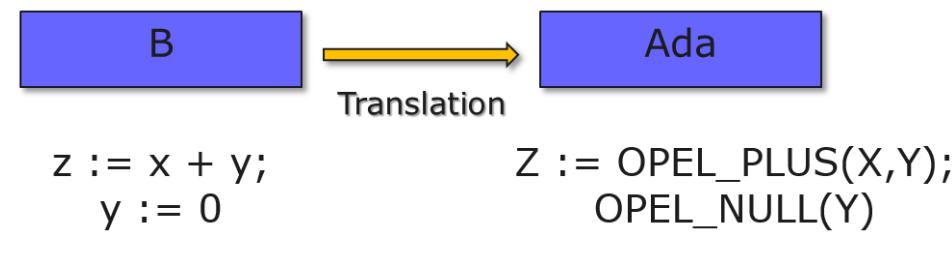
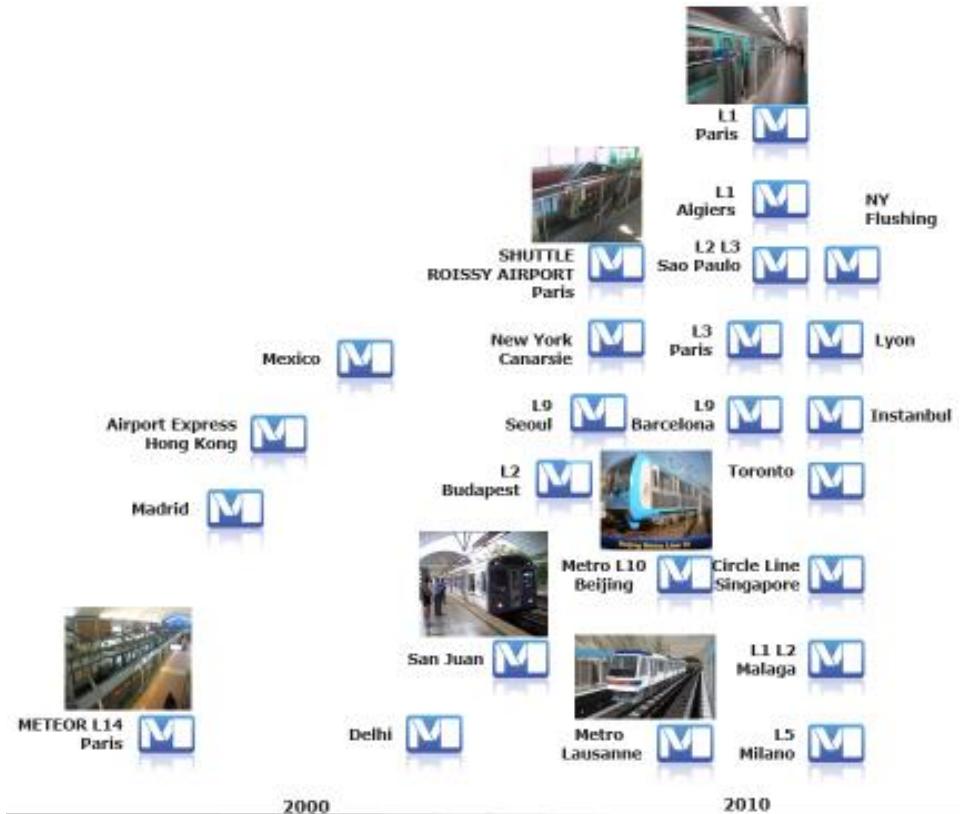
Ada

≡ Long sequence of implementations

- Paris L14 (1998) : 80 kloc
- Paris Roissy Airport Shuttle (2006): 186 kloc onboard, 50 kloc trackside
- Lille (2015): 300 kloc xml compiler

≡ Using different technologies (redundancy)

- encoding (FIDARE): 2 instances
 - inputs, outputs, variables, instructions are encoded
 - the coding key is different for each instance
- diversity (inverse mirror): 2 instances
 - one instance uses big endian model,
 - the other one executes little endian model
- specific hardware (coded secure processor): 1 instance
 - Variables have two fields: value and code. Instructions (OPELS) modified both accordingly. Mismatching value and code indicates a memory corruption.
 - Compensation tables contains tags for all possible path (masks). An unexpected value indicates a program counter corruption



C

≡ Privileged code generation path

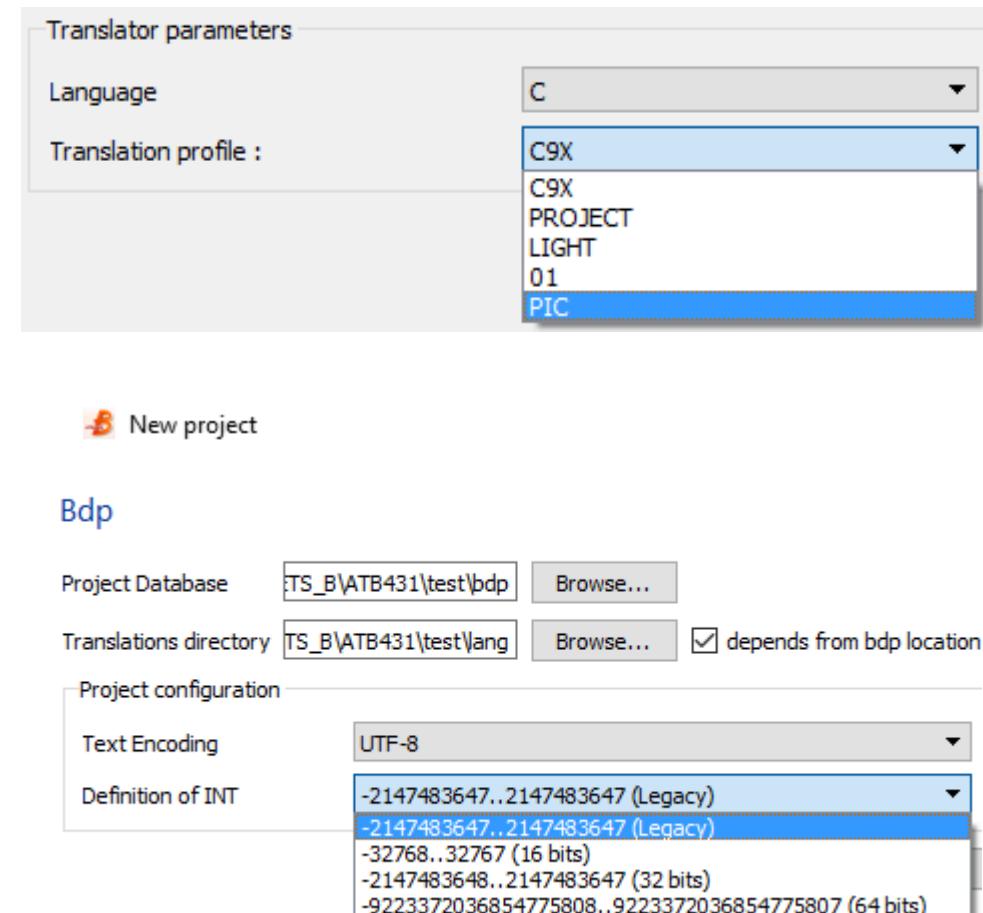
- Code generator that produces:
 - Readable code
 - Compliant with (railways) standards: limited use of pointers
 - Restrictions on accepted B0 (no multi instance)

≡ Modes

- Code generation for a:
 - Machine: skeleton for the component
 - Implementation: code for the component
 - Project: makefile and code for the components
- Profiles:
 - Code generation is highly dependant on the target
 - Predefined translation profiles allow adapt generated code

≡ INT

- INT can be redefined at project level to adapt to algorithm precision



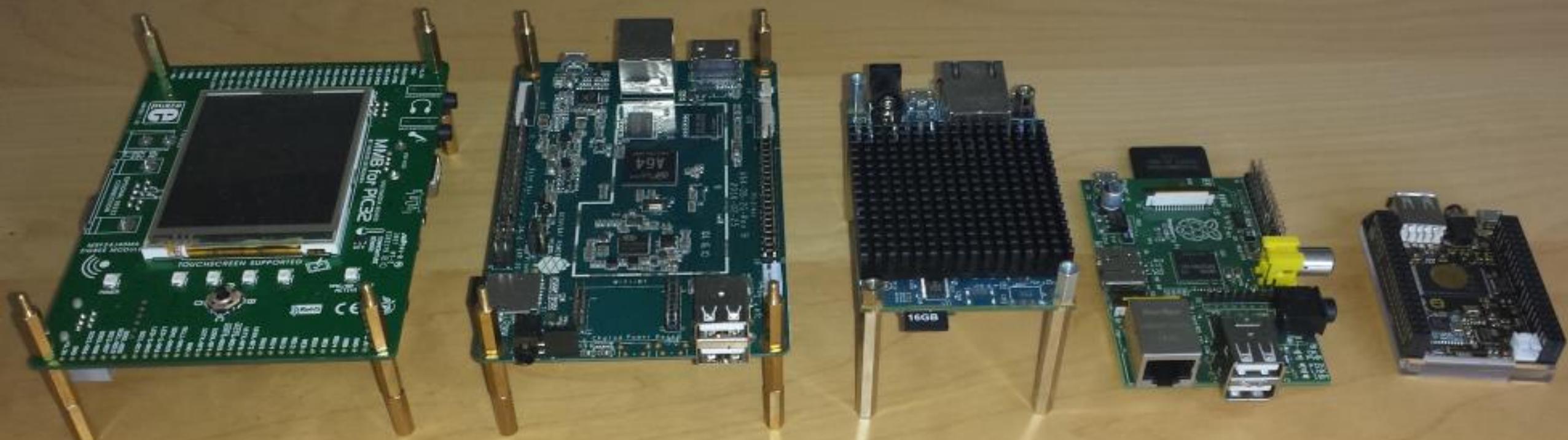
≡ Applications

- C code embedded at Sao Paulo L15 and Stockholm Citybanan



≡ Embedded systems

- Aimed at low cost hardware (from 6€ to 100€)
- Resources available in the future at <https://github.com/TProver/TRBM>: Training Resources for the B Method



MicroChip PIC32

Pine 64

Parallel

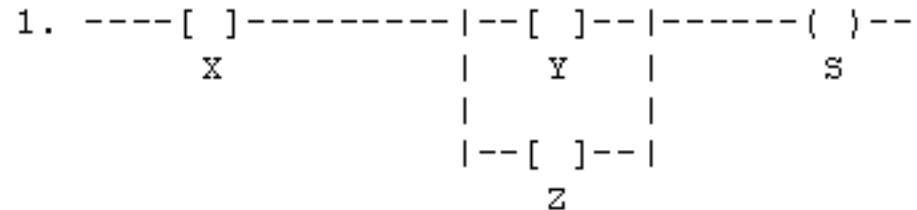
Raspberry Pi

CHIP

Ladder

≡ Programming PLCs

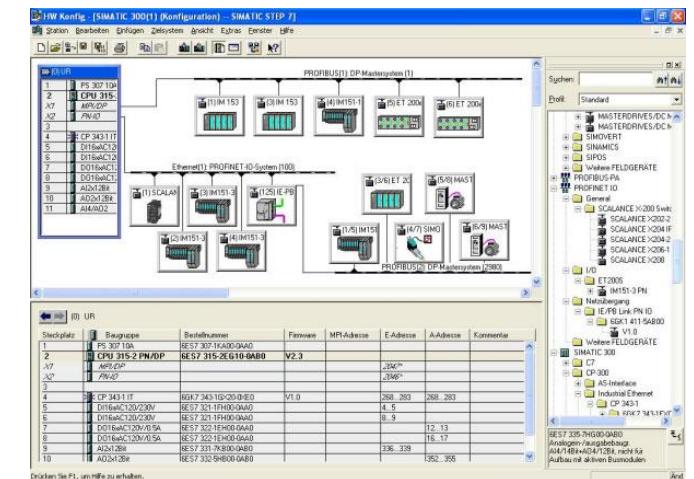
- One language (out of 5) for programming PLCs (IEC61131-3)
- Very Similar to electric circuits



The above realises the function: $S = X \text{ AND } (Y \text{ OR } Z)$

≡ Mandatory IDE

- Step7 IDE required to program Siemens-S7 to keep the SIL3 certificate
- Ladder code generator is not connected to Step7
- Ladder programs have to be manually entered into Step7 with the GUI
- Cross-read required to check identity between programs
- Solution abandonned
- Translator not published because too specific



Instruction List

≡ Programming PLCs

- One language (out of 5) for programming PLCs (IEC61131-3)
- Kind of assembly language for PLCs

≡ Mandatory IDE

- Step7 IDE accept Instruction List copy/paste actions
- Simpler, safer, no further cross-verification
- Translator not published because too specific

≡ Applications

- PSD controller Paris Line 1 (2015), Caracas L2 (2016)
- Bridge Crane Lyon (2013)

```
IMPLEMENTATION T003_set_i
REFINES T_empty_mch
LOCAL_OPERATIONS
    bb <-- ope_01(nn) =
PRE
    bb : BOOL &
    nn : NAT
THEN
    skip
END
OPERATIONS
    bb <-- ope_01 (nn) =
BEGIN
    IF nn=3
    THEN
        bb := FALSE
    END
END
```

```
END
```



```
VAR_INPUT
    nn : INT;
END_VAR

VAR_OUTPUT
    bb : BOOL;
END_VAR

VAR_TEMP
END_VAR

BEGIN

NETWORK
TITLE = RESEAU_1
U();
L      #nn;
L      3;
==I   ;
);
NOT  ;
SAVE ;
BEB  ;

NETWORK
TITLE = RESEAU_2
U      "F_GLOBDB".VKE0;
=      #bb;

END_FUNCTION
```

Instruction List

Bridge cranes (SNCF Lyon)

- Safe movements over catenary lines



Ground PLC



Crane PLC

VHDL

≡ Objectives

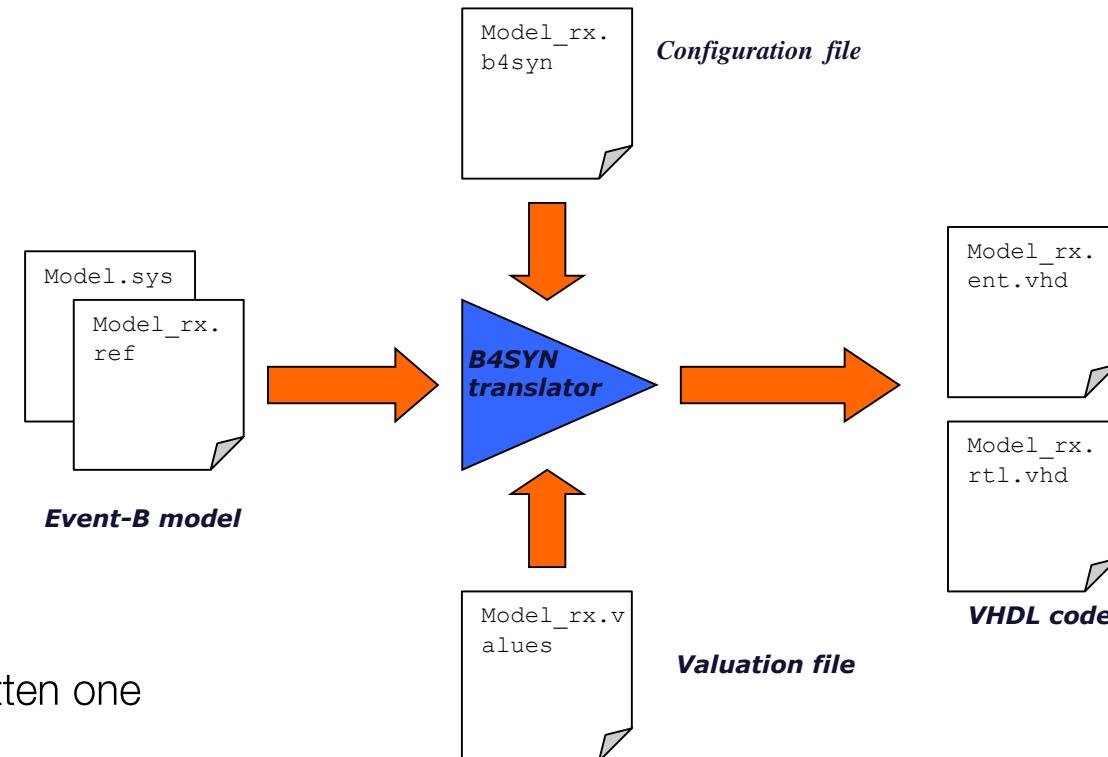
- Code generator producing VHDL from proven Event-B models
- Seamless integration to Atelier B

≡ Development and fine-tuning

- Co-developed with STMicroelectronics Rousset (Smartcard division)
- Event-B model describes synchronous and asynchronous behaviour
- Code generator produces VHDL with a different structure from hand written one
- Applied to smartcard EAL6+ certified product (Memory Protection Unit)
 - Similar size (number of gates), less components, better debug vectors
 - Publication on this subject: *A proved “correct by construction” realistic digital circuit* [1]

≡ Exploitation (B₄SYN)

- Free extension to Atelier B 4.4 (ETA Q4 2016)
- Level crossing controller being developed for French Railways (FPGA, SIL4)



VHDL

≡ Event-B model

Constants

Variables

Events

≡ Parameters

Constants

Variables

- **reset**
- **clock**
- **inputs**
- **combinatorial outputs**
- **synchronous outputs**

Events

- **reset**
- **phi (input acquisition)**
- **psi (combinatorial propagation)**
- **update registers and synchronous outputs**

≡ Event-B model

Constants

- **bit level operation**

Variables

- **reset**
- **clock**
- **inputs**
- **combinatorial outputs**
- **synchronous outputs**

Events

- **reset**
- **phi (input acquisition)**
- **psi (combinatorial propagation)**
- **update registers and synchronous outputs**

Prove the non-divergence of new events (**VARIANT clause**)

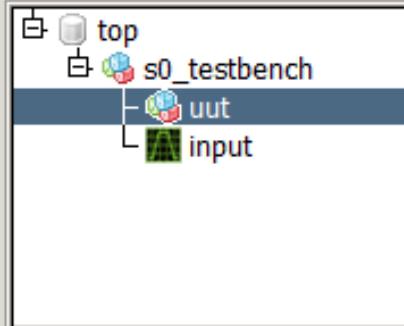
Prove coverage

Prove exclusivity

File Edit Search Time Markers View Help

From: 0 sec To: 145 ns Marker: -- Cursor: 65700 ps

SST



Signals

Time
c1input[2:0]
grd_phi

grd_synchro

c1_in
b1_inb2_in
b3_tb2_t
b1_treset
phi1b1
b2

Signals

b1_in

b2_in

b3_t

b2_t

b1_t

c1

reset

phi1

b1

b2

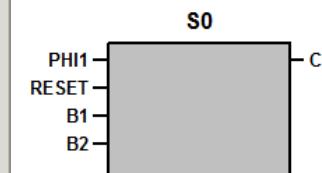
Filter:

Append Insert Replace

Waves

Time
0 10 ns 20 ns 30 ns 40 ns 50 ns 60 nsU
000 010 001 011 111

grd_phi

c1_in
b1_inb2_in
b3_tb2_t
b1_treset
phi1b1
b2

≡ Objectives

- Code generator producing LLVM Internal Representation (IR) from proven B models
- LLVM IR to be translated in any language supported by LLVM (JS, Java, C, Ada, etc.)
- Seamless integration to Atelier B

≡ Development and fine-tuning

- Co-developed with UFRN (Brazil)
- B model describes software functions (no interrupt, no parallel execution)
- Code generator supports C₄B B language subset
- Proof of concept demonstrated on several existing SIL4 software

≡ Exploitation (B₂LLVM)

- Free extension to Atelier B 4.4 (ETA Q4 2016)

```

result <-- pow ( numberA , numberB ) =
PRE
    numberA : INT & numberB : INT & numberB : 0 .. MAXINT
THEN
    result := numberA ** numberB
END
  
```

B Specification

```

result <-- pow ( numberA , numberB ) =
BEGIN
    IF numberB >= 0 THEN
        IF numberB = 0 THEN
            result := 1
        ELSIF numberB = 1 THEN
            result := numberA
        ELSE
            VAR ii , exp IN
                ii := 1 ;
                exp := numberA ;
                WHILE ii < numberB DO
                    exp := exp * numberA ;
                    ii := ii + 1
                INVARIANT
                    ii : INT & ii <= numberB & exp <= numberA ** numberB
                VARIANT
                    numberB - ii
                END ;
                result := exp
            END
        END
    END ;
  
```

B Implementation

```

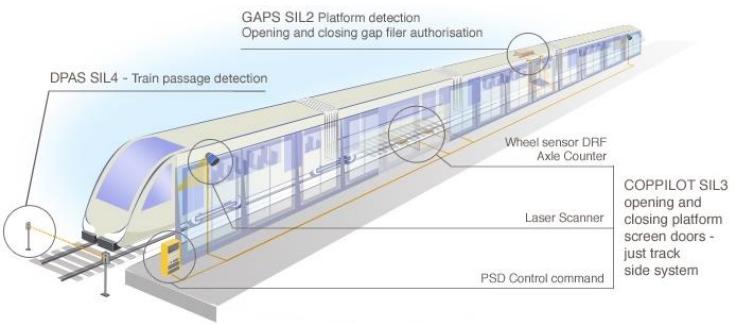
define void @Calculator$pow(i32 %numberA, i32 %numberB, i32* %result) {
entry:
    %ii = alloca i32
    %exp = alloca i32
    %0 = icmp sge i32 %numberB, 0
    br i1 %0, label %label0, label %exit
label0:
    %1 = icmp eq i32 %numberB, 0
    br i1 %1, label %label1, label %label2
label1:
    store i32 1, i32* %result
    br label %exit
label2:
    %2 = icmp eq i32 %numberB, 1
    br i1 %2, label %label3, label %label4
label3:
    store i32 %numberA, i32* %result
    br label %exit
label4:
    store i32 1, i32* %ii
    store i32 %numberA, i32* %exp
    br label %label6
label6:
    %3 = load i32* %ii
    %4 = icmp slt i32 %3, %numberB
    br i1 %4, label %label7, label %label5
label7:
    %5 = load i32* %exp
    %6 = mul i32 %5, %numberA
    store i32 %6, i32* %exp
    %7 = load i32* %ii
    %8 = add i32 %7, 1
    store i32 %8, i32* %ii
    br label %label6
label5:
    %9 = load i32* %exp
    store i32 %9, i32* %result
    br label %exit
exit:
    ret void
}
  
```

LLVM IR code

Binary

≡ C32

- Generate Hex file from B0 implementation
- Application: PSD Sao Paulo L15 (2015), Stockholm Citybanan 2016



Modèle

```

IMPLEMENTATION
    machine_i
REFINES
    machine
OPERATIONS
    operation =
BEGIN
    IF TRUE=TRUE THEN
        skip
    ELSIF TRUE=TRUE THEN
        skip
    ELSE
        skip
    END
END
END

```

Mapping

= 0x00018000	machine_initialisation
= 0x00018028	operation

ASM Mips32

```

1  machine_initialisation:
2      addiu    $sp,$sp,-24
3      sw      $ra,20($sp)
4      sw      $fp,16($sp)
5      movz    $fp,$sp,$zero
6      movz    $sp,$fp,$zero
7      lw      $fp,16($sp)
8      lw      $ra,20($sp)
9      addiu   $sp,$sp,24
10     jr      $ra
11     nop
12     operation:
13     addiu    $sp,$sp,-24
14     sw      $ra,20($sp)
15     sw      $fp,16($sp)
16     movz    $fp,$sp,$zero
17     .if_begin_1:
18     lui     $t2,%hi(1)
19     ori     $t2,$t2,%lo(1)
20     lui     $t3,%hi(1)
21     ori     $t3,$t3,%lo(1)
22     xor     $t1,$t2,$t3
23     sltiu   $t1,$t1,1
24     beq    $t1,$zero,%gp_rel_sub_4_div_4(.if_else_1)
25     nop
26     .if_then_1:
27     b      %gp_rel_sub_4_div_4(.if_end_1)
28     nop
29     .if_else_1:
30     .if_begin_2:
31     lui     $t2,%hi(1)
32     ori     $t2,$t2,%lo(1)
33     lui     $t3,%hi(1)
34     ori     $t3,$t3,%lo(1)
35     xor     $t1,$t2,$t3
36     sltiu   $t1,$t1,1
37     beq    $t1,$zero,%gp_rel_sub_4_div_4(.if_else_2)
38     nop
39     .if_then_2:
40     b      %gp_rel_sub_4_div_4(.if_end_2)
41     nop
42     .if_else_2:
43     .if_end_2:
44     .if_end_1:
45     movz    $sp,$fp,$zero
46     lw      $fp,16($sp)
47     lw      $ra,20($sp)
48     addiu   $sp,$sp,24
49     jr      $ra
50     nop

```

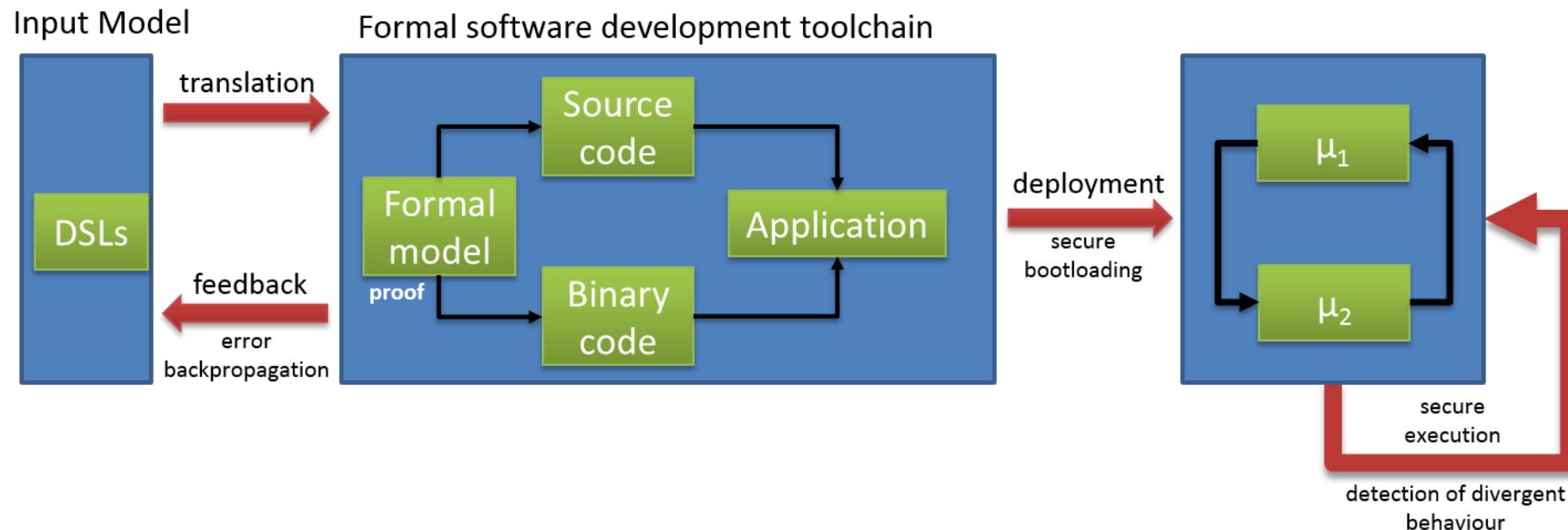
Hex

```

1 : 020000040001f9
2 : 04800000e8ffbd27b1
3 : 048004001400bfaff6
4 : 048008001000beaff7
5 : 0480c000af0a003d3
6 : 048010000ae8c003b7
7 : 048014001000be8fb0
8 : 048018001400bf8f02
9 : 04801c001800bd2764
10: 04802000800e00371
11: 048024000000000058
12: 04802800e8ffbd2789
13: 04802c001400bfafce
14: 048030001000beacf
15: 048034000af0a003ab
16: 048038000000a3cf
17: 04803c0001004a35c0
18: 048040000000b3cf5
19: 0480440001006b3597
20: 048048026484b017a
21: 04804c000100292dd9
22: 0480500003002011f8
23: 04805400000000028
24: 048058000b0001009
25: 04805c00000000020
26: 048060000000a3cd6
27: 0480640001004a3598
28: 048068000000b3cc
29: 04806c0001006b356f
30: 0480700026484b0152
31: 048074000100292db1
32: 0480780003002011d0
33: 04807c000000000000
34: 0480800001000010eb
35: 0480840000000000f8
36: 048088000ae8c0033f
37: 04808c001000be8f93
38: 0480900001400bf8f8a
39: 048094001800bd27ec
40: 048098000800e003f9
41: 04809c0000000000e0
42: 00000001ff
43:
```

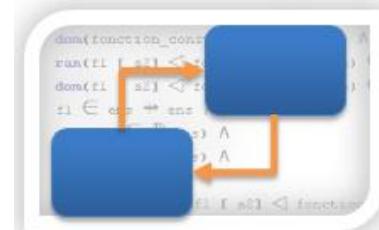
Future

Low Cost High Integrity Platform



≡ Automatic generation of proven code

- Formal part hidden behind the curtain
- Support for bounded algorithm complexity
- Domain Specific Languages: grafcet, relays drawings, etc (IEC61131-3) to keep development perturbation low
- To ease SIL4 certificate achievement:
 - Developer focused on functional aspects
 - Even non high grade engineers could participate

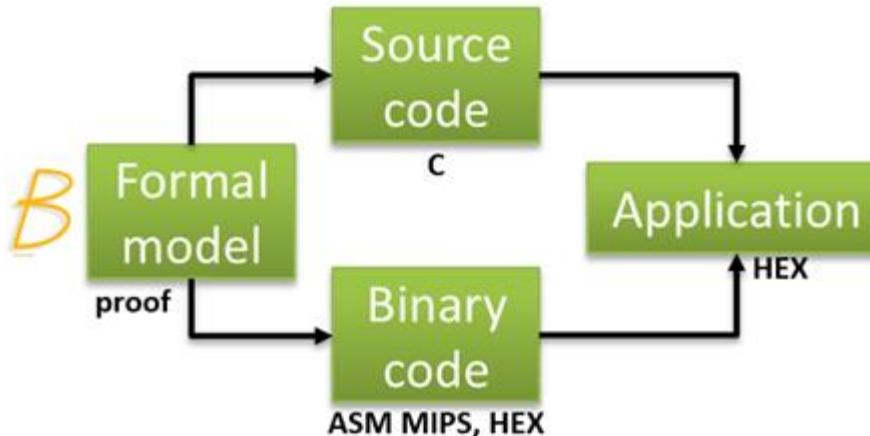


Low Cost High Integrity Platform

≡ 1 B model (application)

- Data
 - Integer arithmetic
 - Boolean equations
 - State machine
 - Variables typing and properties
- Cyclic software, no interrupt modifying state variables

≡ 1 C code generator + commercial compiler => Hex



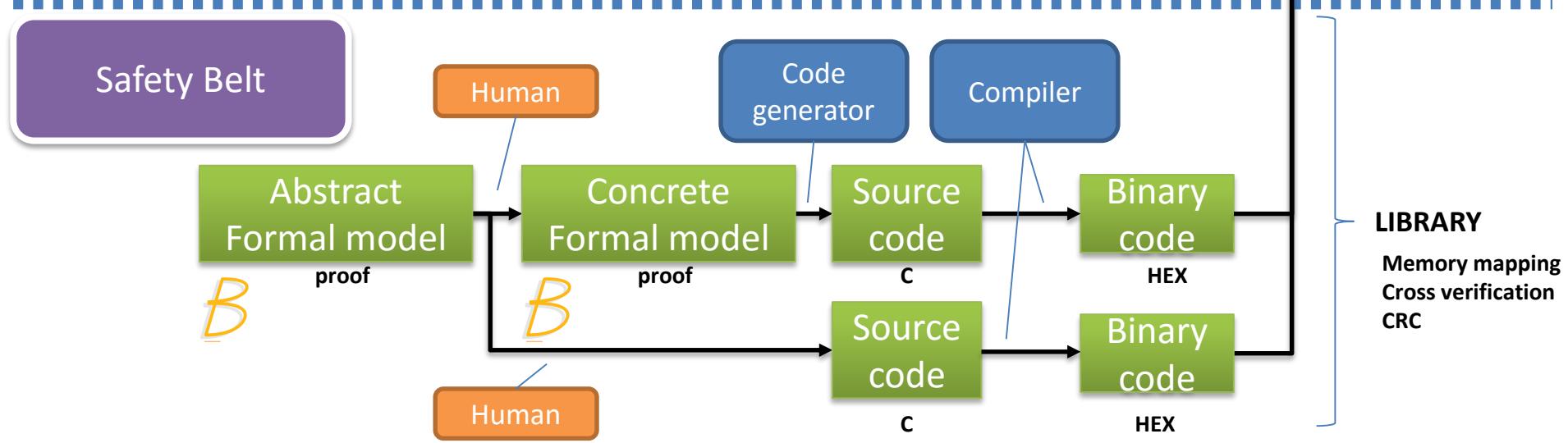
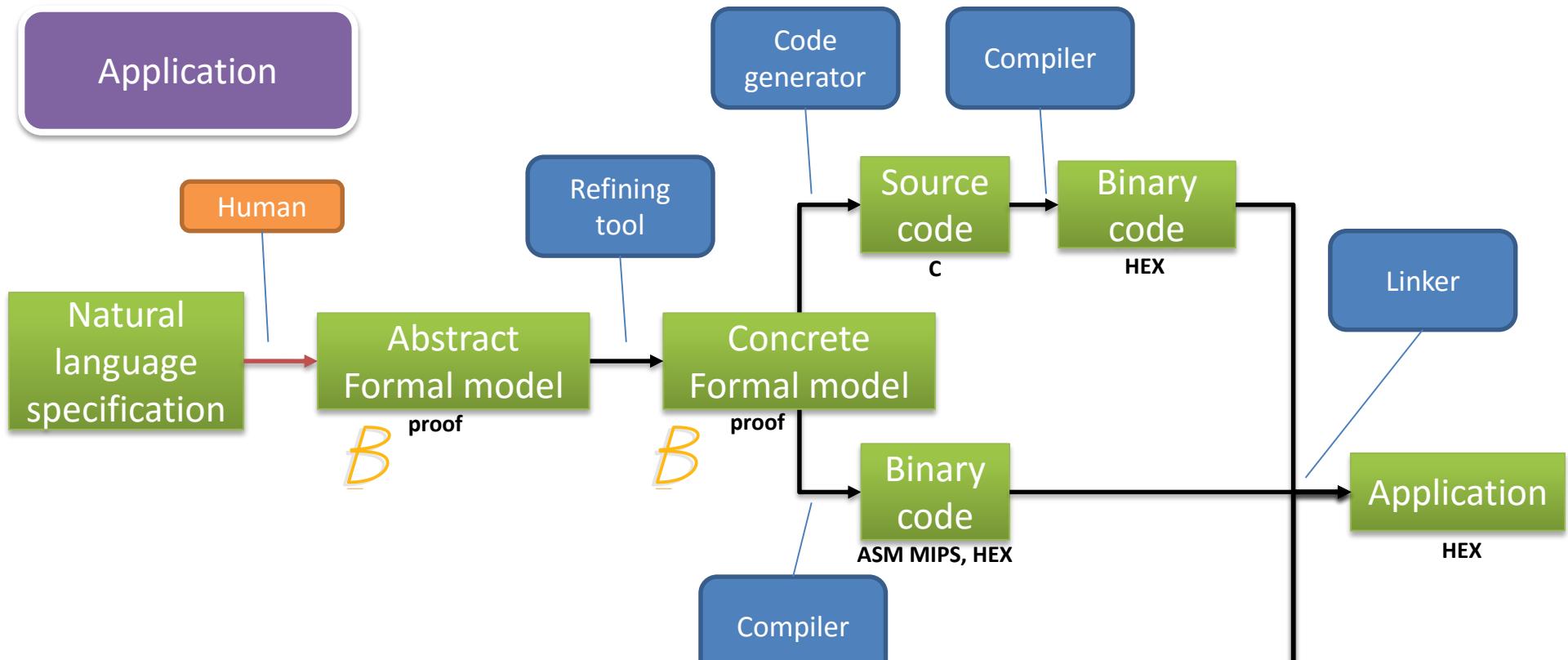
≡ Application proved vs requirements

- Implementation doesn't contradict specification
- A minima, no programming error:
 - overflow,
 - div 0,
 - tables

≡ 1 ASM MIPS / Hex code generator

≡ Low level software ensuring safety developed in B

- Once for all
- Safety features out of reach of the developers
- No requirement to certify the tools



Low Cost High Integrity Platform

≡ Starter-kit @ Q3 2017

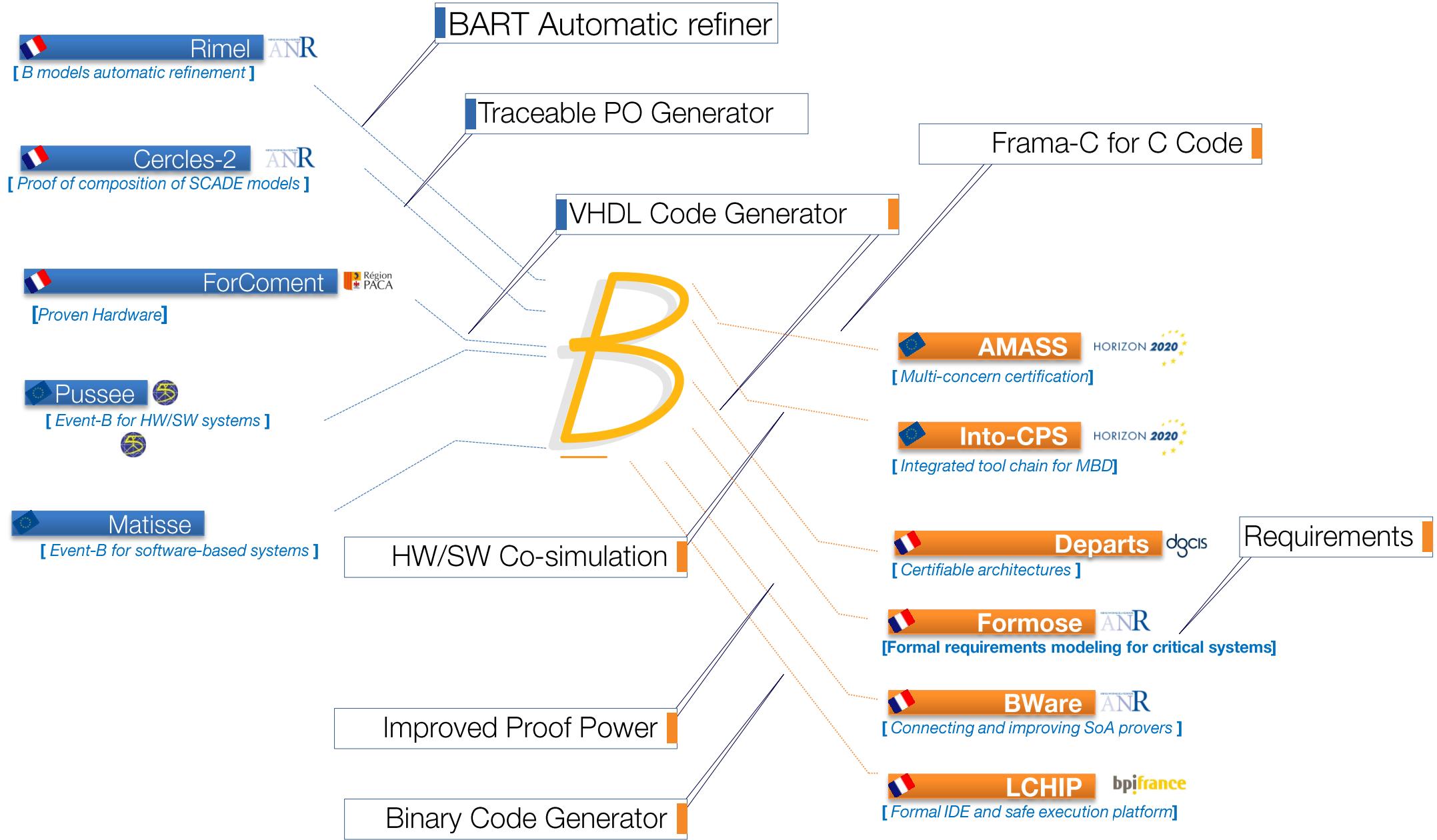
- Mother board (I/Os, maintenance processor, network sockets)
- Daughter card, embedding the double-processor
- IDE v1, based on Atelier B

≡ IDE v2 @ Q2 2018

≡ IDE v3 @ Q2 2019



R&D Projects



Conclusion & Perspectives

- Atelier B still alive
 - +10B passengers transported by « B inside » metros - **Lille 2015, Paris L4 2018**
 - +100M passengers going through doors operated by B software
Sao Paulo L15 2016, Stockholm Citybanan 2017
- Is not only a tool for piloting metros
 - Opening doors safely
 - Validating parameters
 - Contributing to the certification of microcircuits
 - Formal Methods in Safety-Critical Railway Systems*, SBMF 2007
 - Formal Data Validation in the Railways*, SSS 2016
 - A « *Correct by Construction* » *Realistic Digital Circuit*, RIAB/FM 2009
- New usage
 - Integrated to PLC
 - Applications to (nuclear) energy automation
 - Double Processor and Formal Proof for SIL4 Automation*, λμ 2016
 - Formal Virtual Modelling and Data Verification for Supervision Systems*, FM 2015
- Forthcoming evolutions
 - Linked with industrial needs
 - Funded by industrial & collaborative R&D projects
- Let's meet for ABZ 2026 !

formal methods are only a tiny part of the whole picture



Thank you for your attention

Thierry Lecomte |
ABZ 2016
Linz

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